Maas Gilbert Cell Multiplier Measurements
IV: Performance vs. Bias

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1 Overview and summary

We have investigated the Maas multiplier performance as a function of bias voltage as part of the general evaluation program and to find tradeoffs between operation and power consumption. We find that the multipliers work well over a wide bias voltage range with a correspondingly wide range of power dissipations. The dynamic range is highest at the design bias of 10 V. The responsivity is highest at 7 V bias, allowing operation with a slightly reduced dynamic range but less than half of the power dissipation. Operation at even lower biases is possible for inputs with little dynamic range variation. In all cases a simple correction for output stage saturation is possible and useful, and we find that the gain compression can be represented with a hyperbolic tangent shape to a few percent accuracy.

2 Setup

Memo II in this series provides a full description of the measurement setup. Briefly, the measurements here are of a typical chip (characterized in Memo II), mounted on Gel-Pak in the probe station. A 2–18.5 GHz synthesizer and the CW output from a 0.05–40 GHz network analyzer provide the input signals. The synthesizer frequency is 20 to 50 kHz above the nominal frequency. The output signal level is the amplitude of this offset frequency, measured with the "peak find" function of a low-frequency spectrum analyzer. Comparison with an oscilloscope measurement of the peak-to-peak output voltage at a known power level provides the scaling between the spectrum analyzer measurement and responsivities in V/mW. These measurements characterize the device response as an ideal two-tone multiplier: only the level of the fundamental is recorded. At low signal levels the output is a clean sine wave with negligible power in harmonics, but power in the harmonics increases as the multiplier saturates.

The multiplier chip for these measurements was found to be "typical" in earlier measurements for Memo II. In addition, we repeated the measurements for a second "typical" chip, with excellent agreement with the results reported below. Results from the chip mounted in the microstrip high-frequency test fixture (Memo III) generally agree with those here but differ in detail. The detailed differences are in responsivity and noise as well as their behavior with bias. Assigning the discrepancy to individual chips or the mounting structure awaits fabrication of more microstrip test fixtures.

3 Device performance as a function of bias

3.1 Power dissipation

From 3.5 to 10 V bias, the multiplier's power dissipation is closely

$$P = \mathrm{V}_{bias}\left(3.12\mathrm{V}_{bias} - 4.81\right), \quad (1)$$

with V_{bias} in volts and P in mW. At the design bias of 10 V each chip dissipates about 266 mW. At 7 V each chip dissipates about 119 mW, or 45% of the power at a 10 V bias; at 5 V, 53 mW, or 20% of the power at a 10 V bias.

3.2 Responsivity and noise

The top panels in Figure 1 show 4 GHz responsivity and noise variations with bias. The responsivity peaks near 7 V bias, while the noise drops, slowly at first and then faster, with decreasing bias voltage. The bottom panels of Figure 1 are the noise-to-responsivity ratio plotted on log and linear scales. This ratio is interesting because it sets the minimum input signal power level through

$$P_{in} = \frac{3S_V\sqrt{B}}{R} \quad (2)$$

(Memo II), where S_V is the multiplier voltage noise density in $\mathrm{V_{rms}}/\sqrt{\mathrm{Hz}}$, B is the input noise bandwidth in GHz, and R is the multiplier responsivity in V/W. The data in Figure 1 show that there is no noise penalty to operating at lower bias voltages than the 10 V design bias. At maximum responsivity near 7 V, where the multiplier gain is least sensitive to small changes in bias voltage, the minimum input power level is 1.8 dB smaller than it is at 10 V (–22.3 dBm vs. –20.5 dBm for B = 16 GHz).

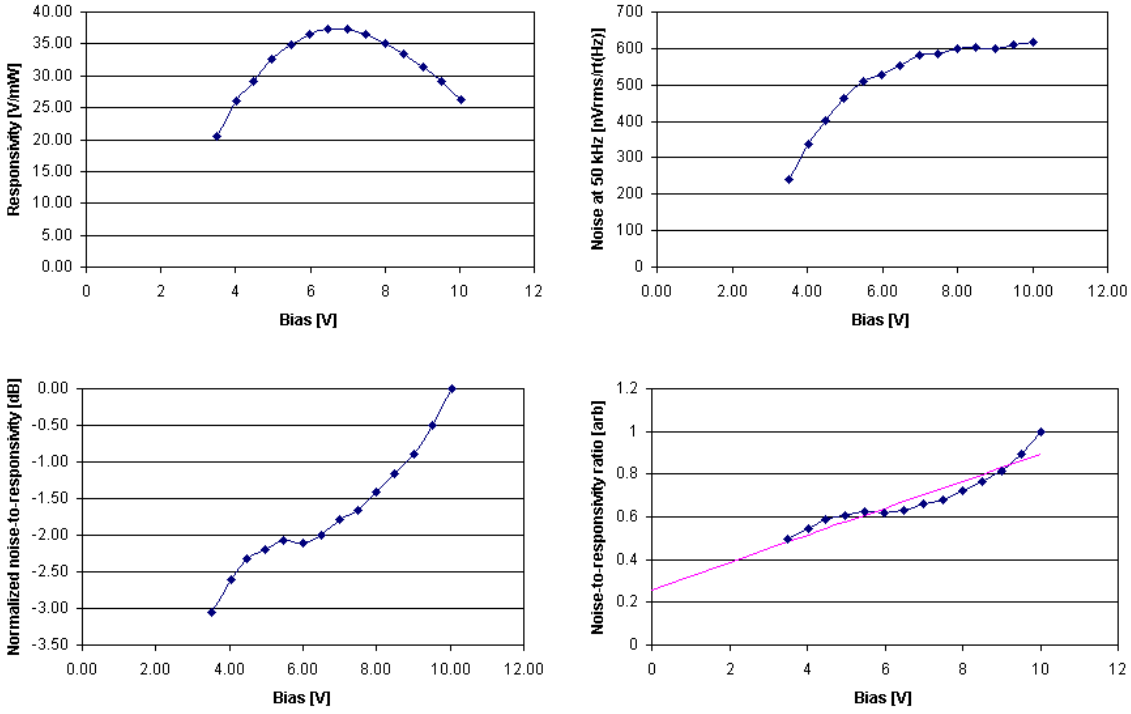

Figure 1: Variation of response, noise, and noise-to-response ratio (on log and linear scales) as a function of bias voltage.

3.3 Linearity and saturation

Operating at lower bias and input power levels is not quite equivalent to operation at the design bias for all applications, however: the compression point falls slightly faster than the input noise-to-responsivity ratio, reducing the input signal dynamic range. Figure 2 contains the large-signal multiplier saturation behavior for 10 V (circles) and 7 V (squares) biases. Higher responsivity at 7 V is easy to see at low input power levels, where the 7 V curve has a steeper slope, but the curve turns over more rapidly with increasing power as the output saturates.

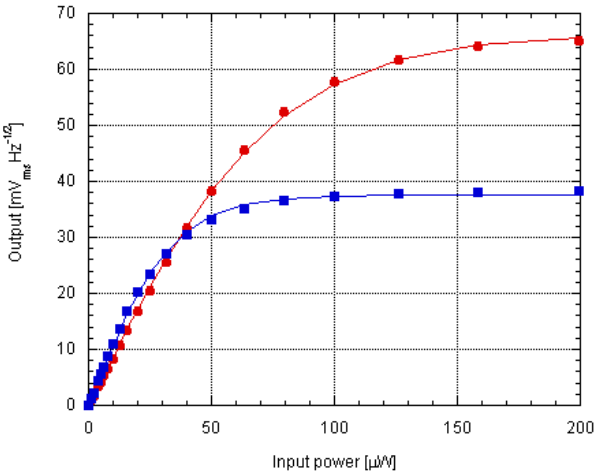

Figure 2: Responsivity vs. input power for 10 V (circles) and 7 V (squares). The solid lines are best-fit hyperbolic tangent curves.

Figure 3 shows the saturation compared with a linear fit to the low-power points. As some measure of the linear regime, the 1 dB compression point is at –11 dBm input power at both inputs for a 10 V bias, and at –14.5 dBm for 7 V bias. Since the minimum signal level is lower by 1.8 dB for 7 V bias, this difference corresponds to an approximate 1.7 dB loss in dynamic range at the lower bias.

Neither of these levels are very large compared with the minimum power levels given by equation (2) of –20.5 and –22.3 dBm, however, so some saturation will be present in most applications, particularly those involving noise signals. Correcting for saturation in software is reasonable for many applications if even an approximate saturation law is available. The solid lines in Figure 2 are results from a simple hyperbolic tangent gain compression fit, with Figure 4 showing that the fit is good within two percent at any level where a compression correction would be significant. The low-level gain of the Gilbert cells should be proportional to $\tanh^2(\sqrt{P_{in}})$, but the voltage swing compared with the output DC offset shows that the compression here is clearly in the output stages and not in the cell itself. Allowing corrections to 3 dB compression from a linear device increases the upper power level to about –8 dBm for 10 V bias (12.5 dB dynamic range) and –11.5 dBm for 7 V (11 dB dynamic range). The coefficients in the curve fit will change for compression by broadband noise, but the functional form should still be close.

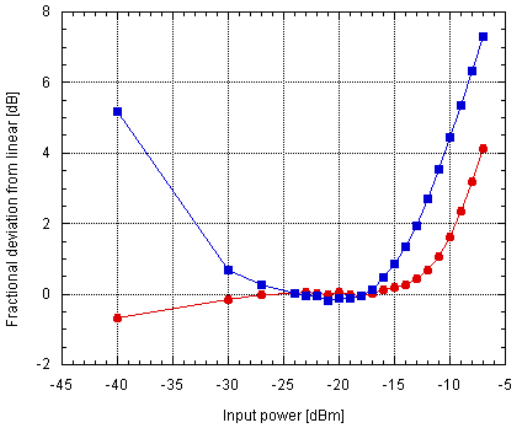

Figure 3: Responsivity fractional deviation from a linear fit in the low-input-power region for 10 V (circles) and 7 V (squares) bias.

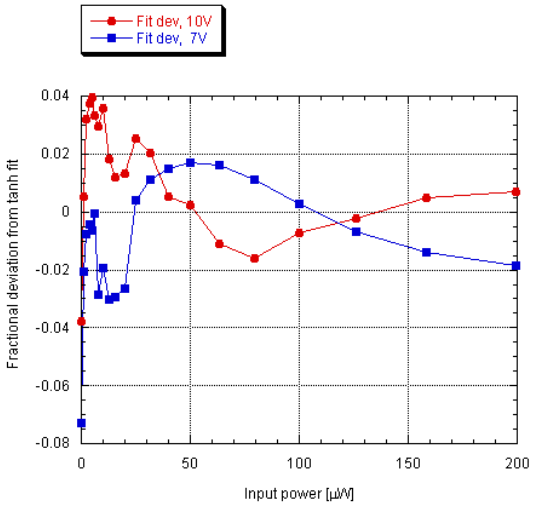

Figure 4: Responsivity fractional deviation from the tanh fit for 10 V (circles) and 7 V (squares) bias.

3.4 Responsivity vs. frequency

All of the discussion above is based on data taken at 4 GHz, the peak of the responsivity-vs.-frequency curve. Figure 5 shows that the responsivity increase is nearly flat with frequency across at least the 2 to 18 GHz band. The responsivity is slightly higher from 8 to 16 GHz at the lower bias.

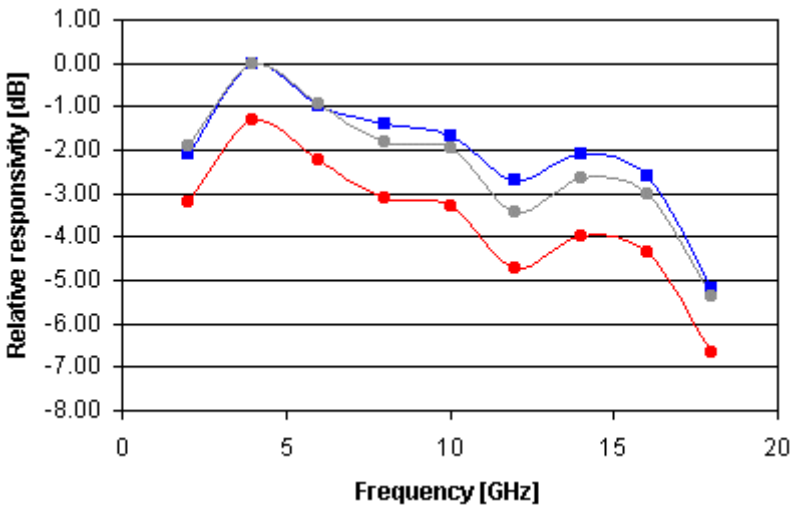

Figure 5: Relative responsivity vs. frequency for 10 V (bottom curve, circles) and 7 V (top curve, squares) at –25 dBm (3 µW) input power. The intermediate curve shows data from the 10 V case shifted by 1.3 dB to match the responsivity of the multiplier at 4 GHz and 7 V bias.