Ultra-wideband Microwave Spectrometers for Heterodyne Spectroscopy: Year Two Project Summary

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1 Summary

This project is on schedule and within budget, due in large part to the delivery and successful operation of the first batch of prototype multiplier and test structure MMICs in December 2001. The main goal of this work is to develop advanced circuit components for correlation spectrometers and detectors with bandwidths of approximately 2—18 GHz. We report here on first tests from custom MMIC (monolithic microwave integrated circuit) multiplier prototypes and wideband power dividers. Devices from our first batch of MMICs work well, a nice success on the first run. This brings the timeline back to plan by making up for last year's schedule slip caused by the difficulty of finding a semiconductor foundry willing to work on a development project rather than mass production. Testing in January and February 2002 showed that the devices have a 3 dB bandwidth from 2 to 16 GHz, only slightly narrower than the goal, and noise levels that are suitable for astronomical applications.

2 MMIC test wafer run

We held a formal design review of the multiplier circuit, additional test structures, and testing plan in the Electrical Engineering Department at Caltech in August 2001. We received very useful comments from the attendees and our advisors, in particular S. Weinreb.

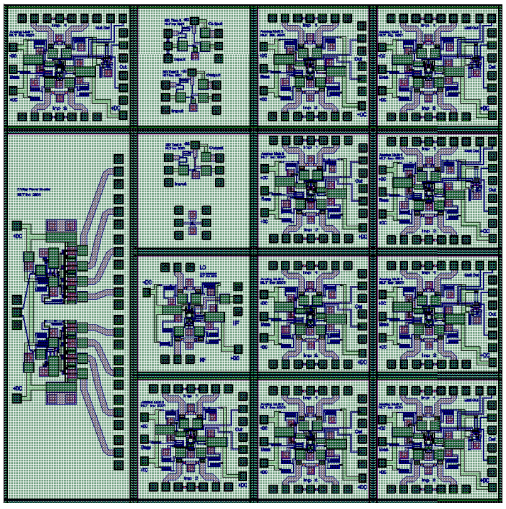

Figure 1: Drawing of the test field reticle containing multipliers, test structures, and an 8-way active power divider. The reticle size is 6 by 6 mm.

After discussion with the foundry, Global Communications Semiconductors, we decided that a shared wafer run would be a sensible approach; this would yield fewer devices, but the possibility of returning for a second fabrication within our budget. The design was finished in October and devices delivered in December 2001. Figure 1 is an image of the reticle for the test field, a 6 by 6 mm area containing two multiplier variants, a variety of test structures, and an 8-way active power divider. The transistors are InGaP HBTs with specified f_T of 100 GHz.

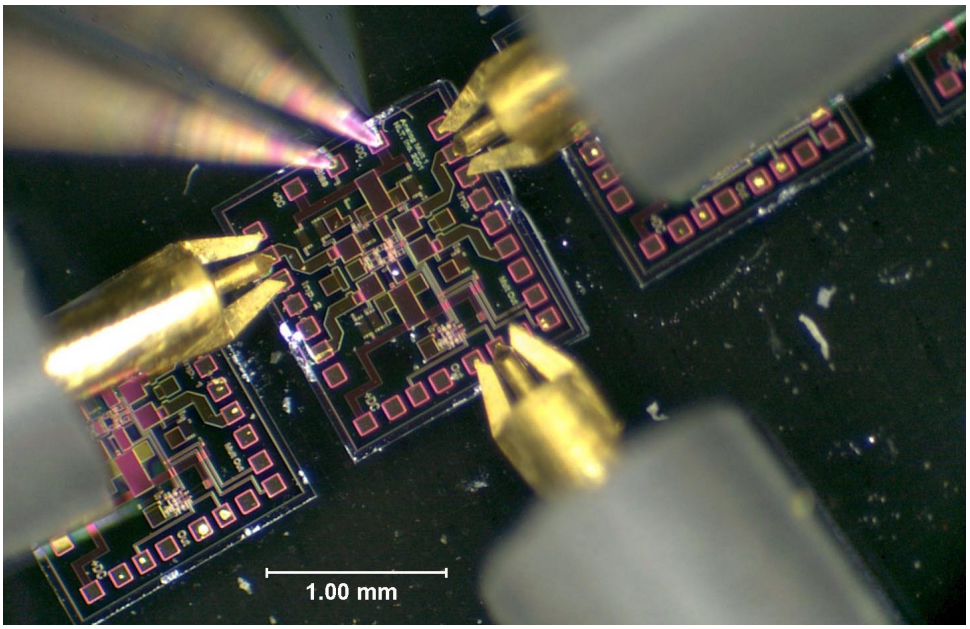

Figure 2: View of test chips with microwave and DC bias probes.

Figure 2 shows a multiplier chip during testing in a microwave probe station in the lab at the University of Maryland. Initial tests of the two multiplier circuits with different bias conditions identified the operating mode with the best responsivity-to-output noise ratio: the chip with integrated postamplifier and the low power dissipation bias condition. Power dissipation in this mode is 256 mW per device, or less than 18 mW/GHz. It is possible to reduce the power dissipation to 165 mW by using the chip without the postamplifier. This decreases the output signal by a factor of forty and decreases the responsivity-to-output noise ratio by a factor of four.

Figure 3 shows the normalized response of the multiplier versus frequency, showing a 3 dB bandwidth from about 2 to 16 GHz. The bandwidth, while adequate for this project, is lower than expected. Analysis of preliminary data from the test amplifiers on the reticle indicate that f_T may be 70 GHz instead of the 100 GHz specified by the foundry. We are refining and complementing these measurements and will consult with the factory about a full or partial makeup run if the devices do not match specifications. Faster transistors should improve the response at the high end of the band. The peak responsivity is 29 V/mW for input power levels of –25 dBm at both inputs. Significant

gain compression appears at power levels of about –13 dBm as the output voltage swings close to the positive rail.

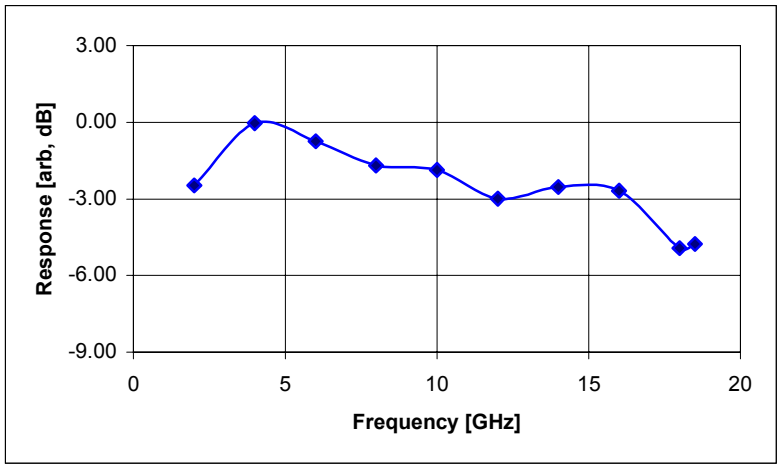

Figure 3: Average normalized response versus frequency for the sample of eight multipliers. The peak response in this plot is 29 V/mW.

The typical output noise density is about 0.7 $\mu V_{rms}/\sqrt{Hz}$ at 50 kHz, as shown in Figure 4, with the noise power leaving its $1/f$ region by 20 or 30 kHz. Phase switching at frequencies above 30 kHz are appropriate. Figure 5 combines responsivity and noise to find the minimum power level needed to keep the spectrometer noise below 5% of the total system noise. For a 16 GHz bandwidth spectrometer the input power to each device should be approximately –15 to –20 dBm, depending on input frequency, at a 50 kHz phase switch. A 1 ms integration time allows a dynamic range of 6 to 9 dB. These requirements are straightforward to meet with existing hardware.

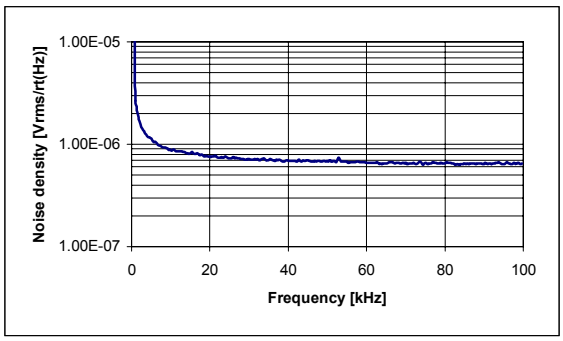

Figure 4: Average output noise versus frequency for the sample of eight multipliers.

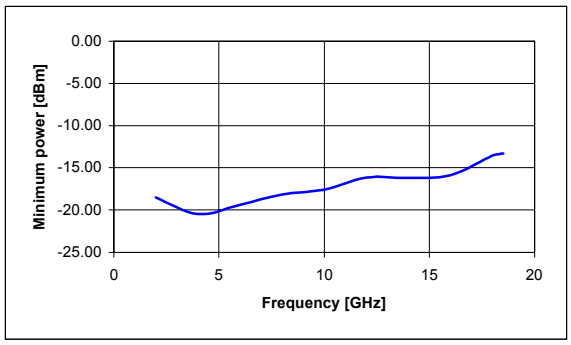

Figure 5: Minimum input power level for a 16 GHz bandwidth input.

Tests of a sample of eight chips indicate about a 1 dB scatter in responsivity and in noise, with good correlation between the two. The average values for response and noise are therefore useful for power level calculations since the two scale together, and all devices have essentially the same requirement on input power for good system noise performance.

3 Power division for multi-lag correlator

Early in the project it became clear that power distribution within a multi-lag correlator was a critical item, not much less important than insuring good multiplier performance. Analysis showed that the power distribution approach we used for the WASP2, resistively tapped delay lines, would not be sensible at the upper end of the band for this project. Even small amounts of stray capacitance shunt current to ground instead of letting it flow through the ~1 kΩ tap resistors and into the multipliers. We have taken two approaches for power dividers in this project: an active 8-way divider (see Figure 1), and a 16-way Wilkinson power divider. Figure 6 shows the divider in a test holder. The divider is fabricated in thin-film technology on a 1×1 inch square 10 mil thick alumina substrate. A full electromagnetic model (in AWR Microwave Office) was central to the design. Figure 7 is the measured transmission to the two test ports from 0 to 25 GHz: the divider performs well over the project's 2-18 GHz design goal band and is useful to above 20 GHz. Port reflection coefficients and differential time delays are also acceptable.

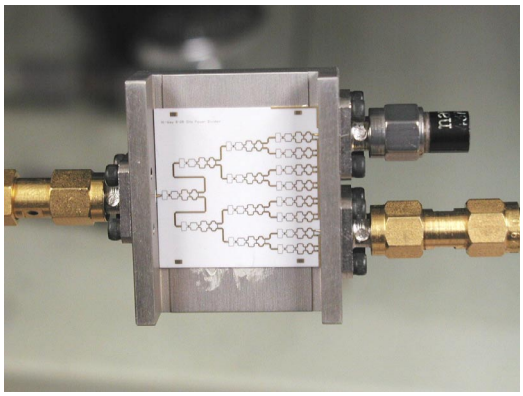

Figure 6: Photograph of 16-way power divider in test holder.

With performance this good, it seems that the passive divider is preferred over the active divider unless space is at a real premium: there is no difficulty with power levels, and the passive device does not add to the power budget.

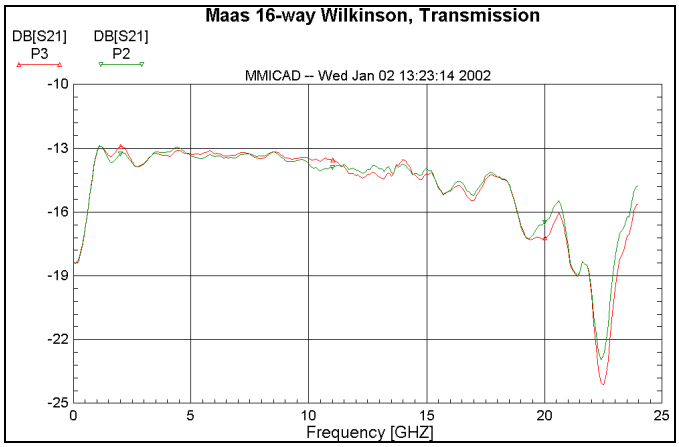

Figure 7: Transmission to two test ports of the 16-way power divider.