SMA/SI Functional Interface: Summary of SMM Tests at CSEM

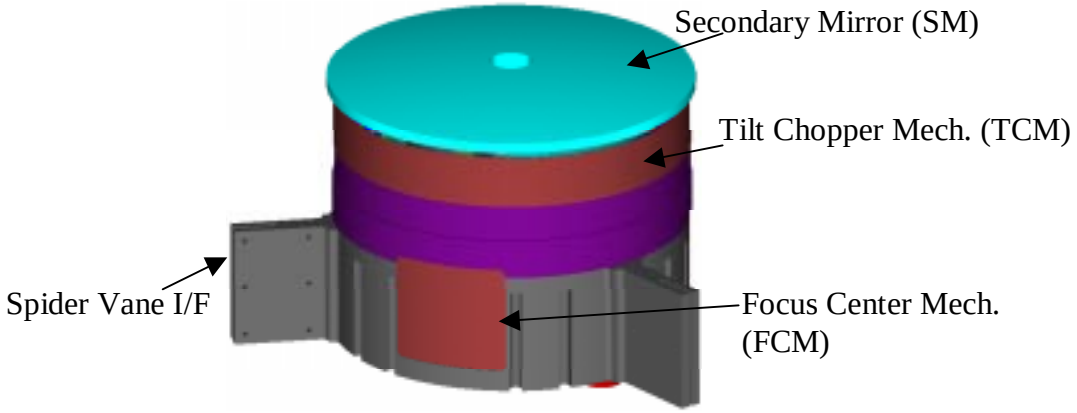
Jackie Davidson

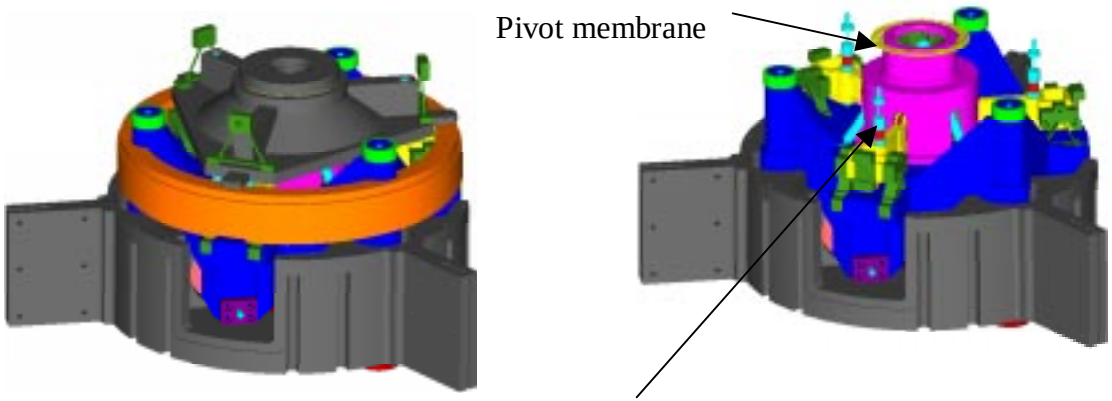
6/27/02; 6/28/02; 7/03/02

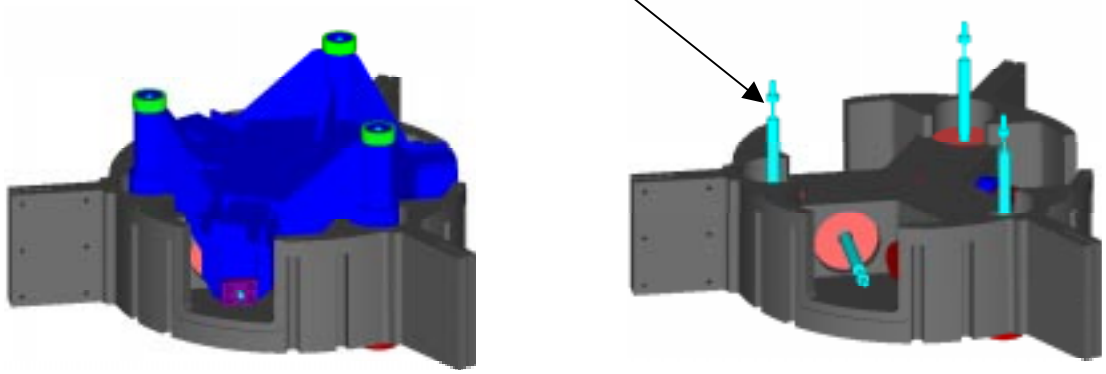
(after Science Support Telecon)

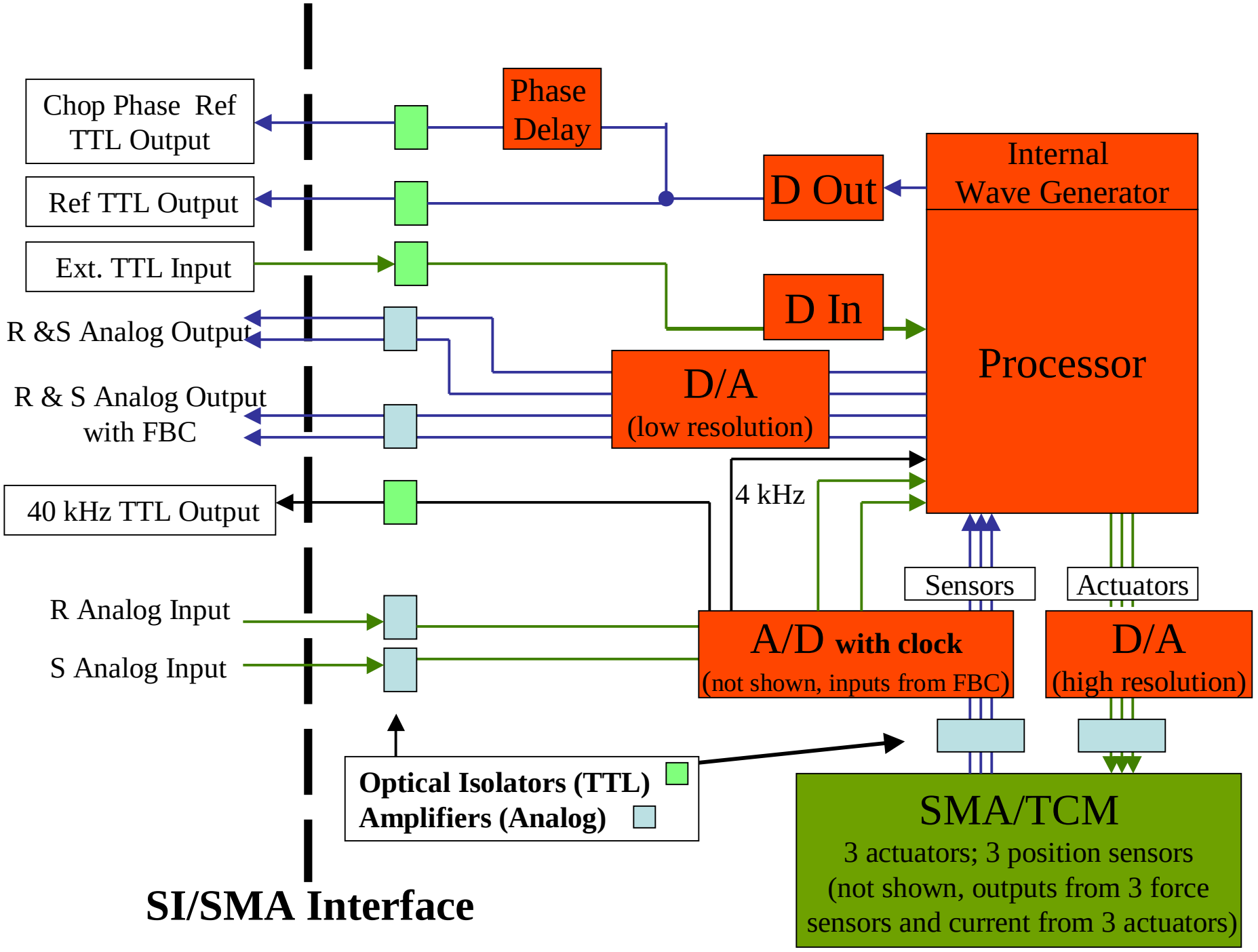
(after further inputs from CSEM)

Recall the SMA hardware







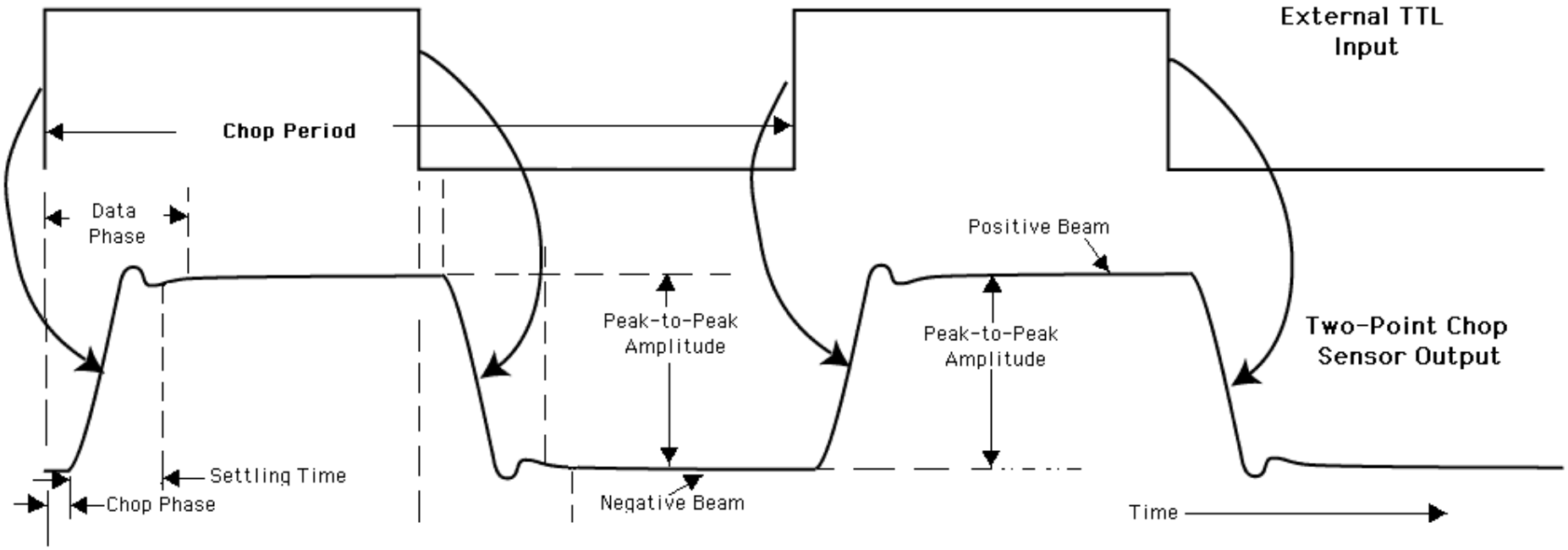

Chop Phase Ref TTL Output
Ref TTL Output
Ext. TTL Input
R &S Analog Output
R & S Analog Output with FBC
40 kHz TTL Output
R Analog Input
S Analog Input
Phase Delay
D Out
D In
D/A (low resolution)
Internal Wave Generator
Processor
4 kHz
Sensors
Actuators
A/D with clock (not shown, inputs from FBC)
D/A (high resolution)
Optical Isolators (TTL)
Amplifiers (Analog)
SMA/TCM
3 actuators; 3 position sensors
(not shown, outputs from 3 force sensors and current from 3 actuators)
SI/SMA Interface

External TTL Synchronization Mode

- SI Commands to MCS when setting up external TTL synch. mode:
  - External mode requested
  - 2-pt or 3-pt chop
  - Amplitude of chop (if 2-pt) or Amp-1 & Amp-2 (if 3-pt)
  - Chop angle desired
  - Chop offset desired
  - Data Phase (or Reference Phase) desired

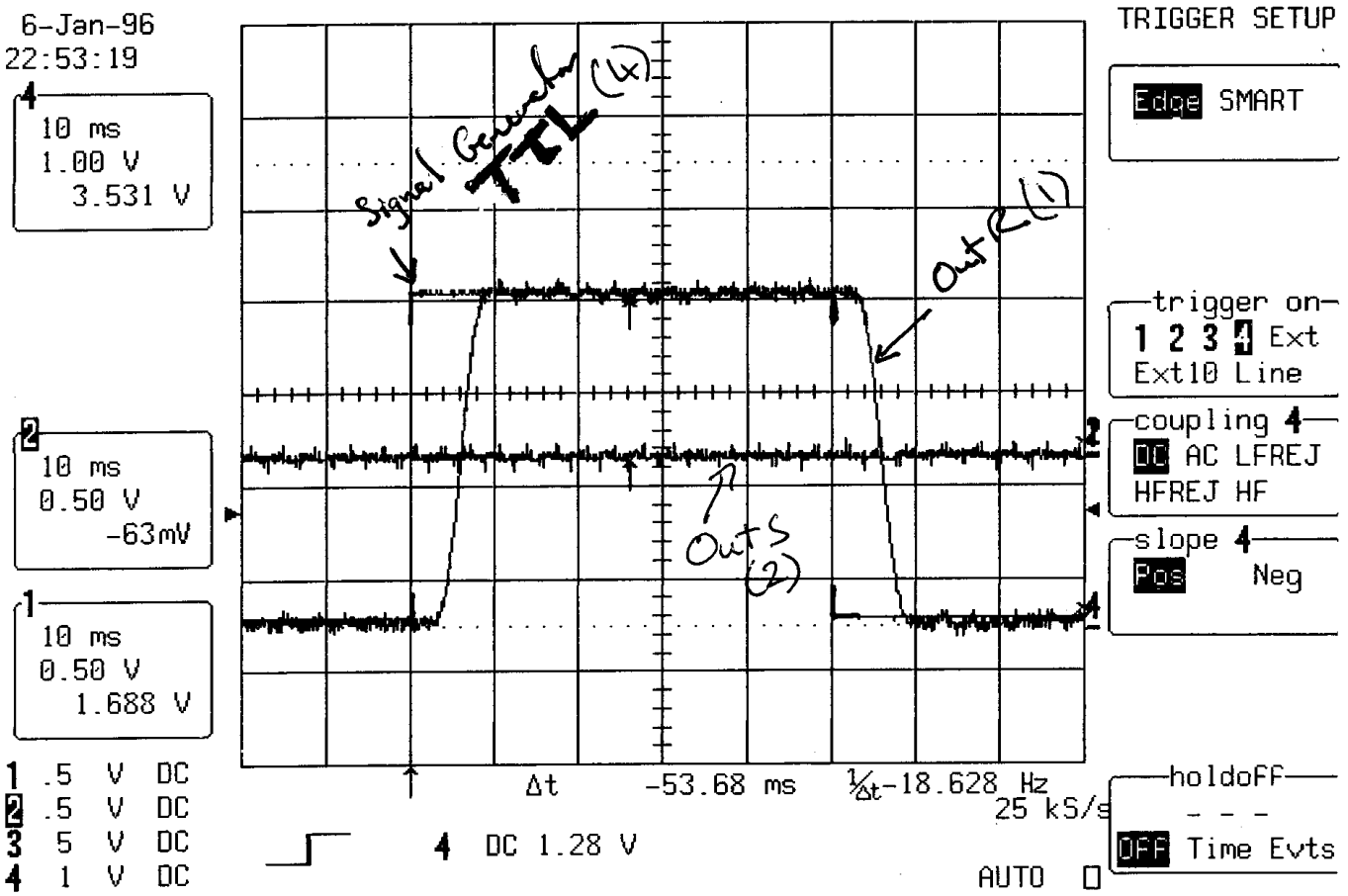
- SI electronics sends a TTL signal to SMA
  - TTL Frequency: $0.5\ \text{Hz} \leq \text{freq} \leq 20\ \text{Hz}$ for 2-pt chop
  - TTL Frequency: $1\ \text{Hz} \leq \text{freq} \leq 20\ \text{Hz}$ for 3-pt chop
    - For 3-pt chop TTL frequency twice the 3-pt chop frequency

External Synch for 2-point Chop

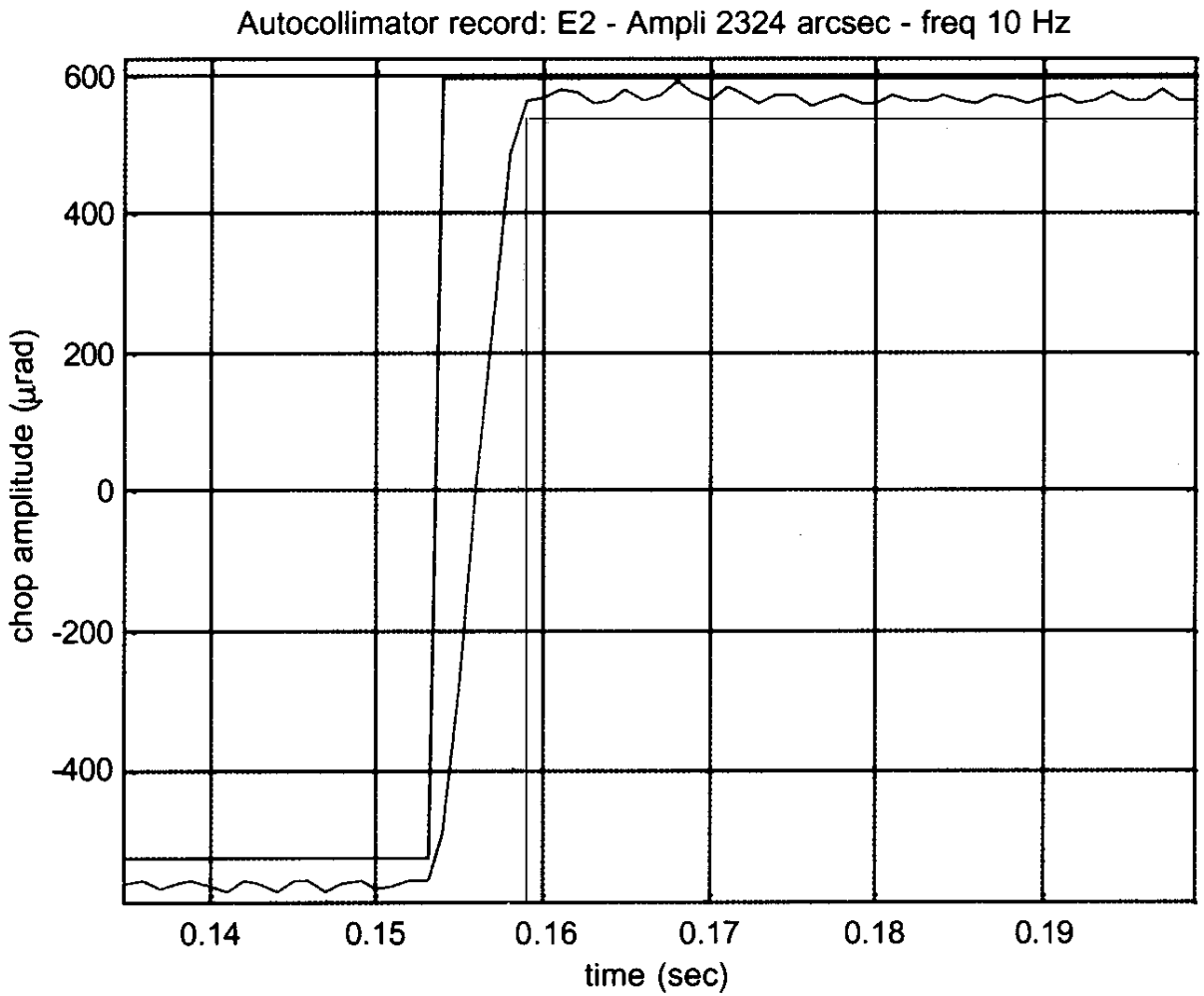


DCR-0106.R1: Polarity phasing between the sync-in TTL signal and the chop directions shall be provided. CSEM states: chopper always starts (or re-starts) with TTL= 1 triggering a positive end-point. After a start, then TTL=0 corresponds to a negative end-point, and TTL=1 a positive end-point. If chopper/synchronization stops for some reason, a “re-start” will automatically force a TTL=1 triggering a positive end-point. No 180 degree phase ambiguity.

Actual 10 Hz external TTL ± 0.5 arcmin chop waveform - Oscilloscope Readout (at 4 kHz)



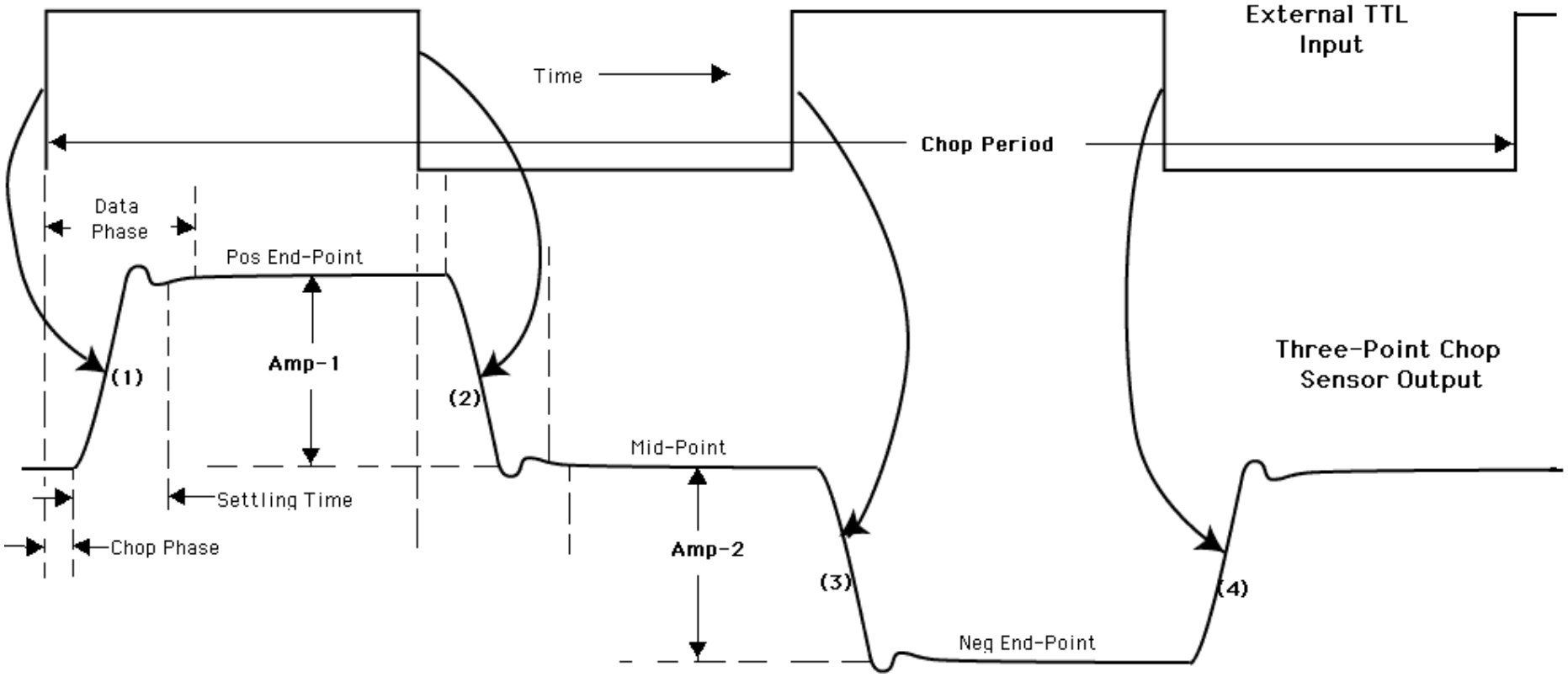
Actual external TTL ± 0.5 arcmin chop waveform - Autocollimator Readout (at 1kHz)



} ±3%

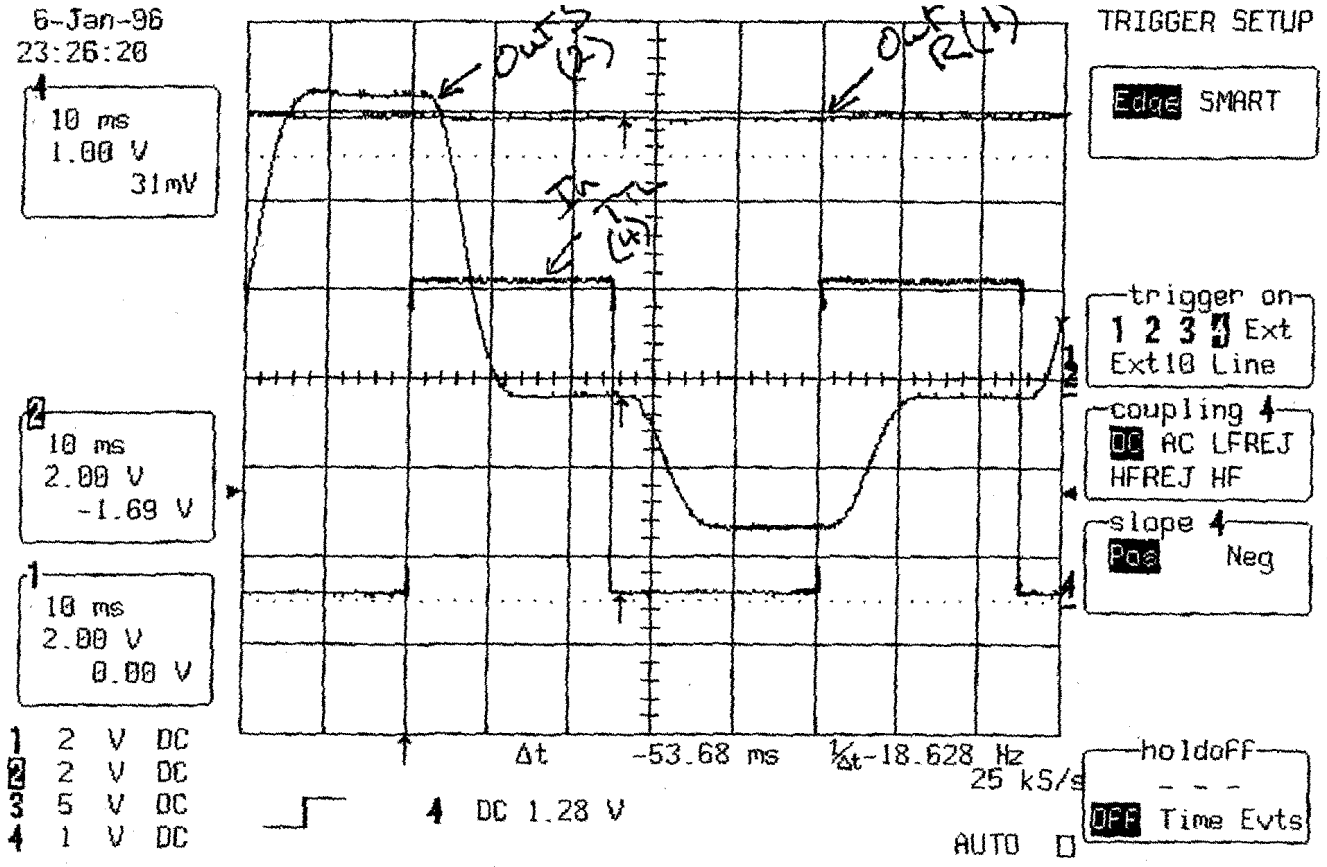
But also see slide 23 in regards to end-point stability for internal chop.

External Synch for 3-point Chop



DCR-0106.R1: Polarity phasing between the sync-in TTL signal and the chop directions shall be provided. CSEM states: chopper always starts (or re-starts) with TTL= 1 triggering a positive end-point. After a start, then TTL=0 always corresponds to a mid-point, and TTL=1 either a positive or negative end-point, depending on the place in the sequence. If chopper/synchronization stops for some reason, a "re-start" will automatically force a TTL=1 triggering a positive end-point.

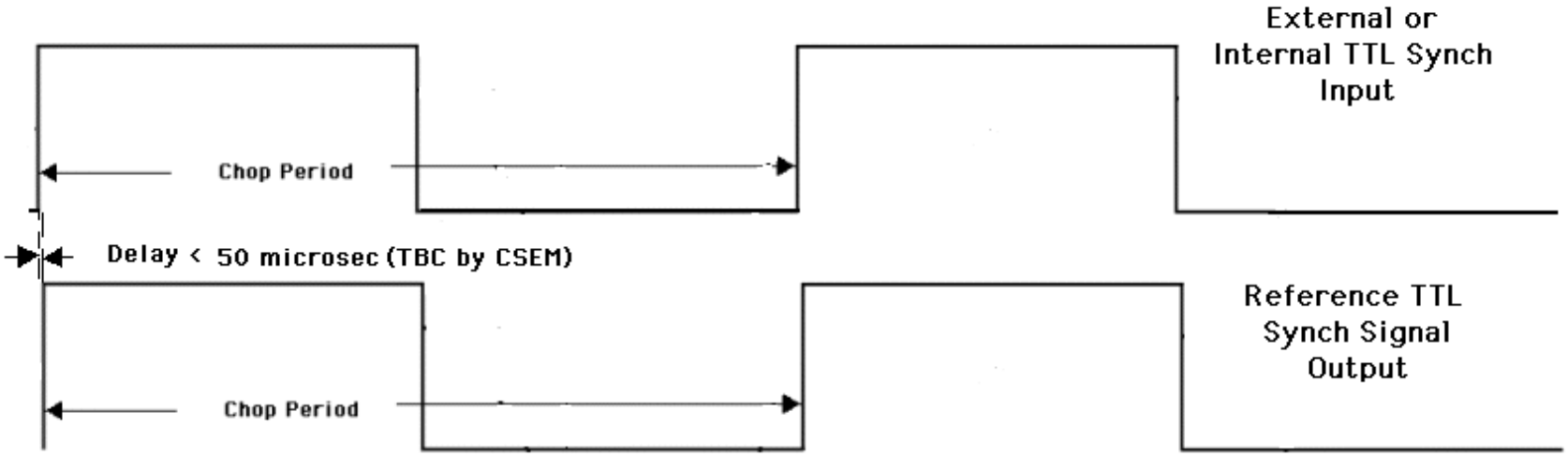
Actual 10 Hz external TTL 3-point chop waveform with [Amp-1= 3.7arcmin] & [Amp-2 = 1.6 arcmin] with R-Axis Chop Offset = 3.2 arcmin



Discussion on Polarity for both 2- and 3-Point Chops

- Casey concerned there is a possibility for a 180 degree phase flip in the present set-up while taking data using external TTL Sync - especially after a re-start.
- CSEM input: Re-starts should not be a problem for 2-point chop, since Ref TTL=1 should always correspond to positive end-point. However, for the 3-point chop, only the mid-point is unambiguous (Ref TTL=0). (Ambiguity of end-points removed only if SI computer can identify "first Ref TTL=1", to identify the positive end-point, when re-start occurs in SMA processor.)
- Dunham points out that the R and S Analog Outputs can be used to check polarity unambiguously if need be.
- Casey urges all SI Teams to monitor, record, and use R and S Analog Outputs with Ref TTL to check polarity while taking data.
- Most on the telecon seemed OK with the current set-up. The desire to have the ability to drive any chop frequency externally (between 0.5 Hz and 20 Hz) and to be able to trigger all chop transitions, over-rides the polarity issue. (The DCR0106.R1 external synchronization algorithm, where only the leading edge of a chop cycle was triggered externally by the leading edge of an external TTL signal, was formulated to assure unambiguous polarity. But this method is not suited to an SMA with internal wave generation restrictions to frequencies of 0.5 Hz to 20 Hz in steps of 0.5 Hz.)

Reference TTL Output



CSEM:

- For Internal TTL

  - Delay ~ 60 microsec (mostly due to one optical isolator; see slide 3)

- For External TTL

  - 116 microsec < Delay < 366 microsec (mostly due to two optical isolators and 250 microsec jitter caused by the 4 kHz sampling limitation of the processor; see next slide.)

Discussion on phase delay between Input TTL (External or Internal) and Ref TTL Output

- SI Teams on the telecon did not worry that the delay between TTL Input and Ref TTL Output greater than 50 microsec (but should not be in millisecs) - BUT the delay must be stable.

- CSEM reports that there is sample jitter if the external TTL input is not synchronized with the 4 kHz SMA clock. SI teams could do this with the 40 kHz clock output. Then the delay would be stable with a value of about 120 microsecs (i.e., two optical isolators).

- The sampling jitter is transferred to the Ref TTL Output and chop waveform to the SMA actuators, so the Ref TTL Output jitter due to "sampling jitter" should be in phase with the R & S Output jitter due to "sampling jitter".

Chop Phase Stability
(as measured by CSEM using R & S Analog Outputs)

- Phase stability with Internal Sync

Chop Frequency (1/ **T**chop) in Hz	Jitter (**δ**jitter) in µsec	**φ**stab in degrees
1	100	0.036
5.5	100	0.2
7	100	0.25
20	100	0.72

- Phase stability with External Sync

Chop Frequency (1/ **T**chop) in Hz	Jitter (**δ**jitter) in µsec	**φ**stab in degrees
1	330	0.12
5.5	330	0.65
7	330	0.83
20	330	2.4

- Phase stability with External Analog Waveform (square wave)

Chop Frequency (1/ **T**chop) in Hz	Jitter (**δ**jitter) in µsec	**φ**stab in degrees
1	200	0.072
5.5	200	0.4
7	200	0.5
20	200	1.44

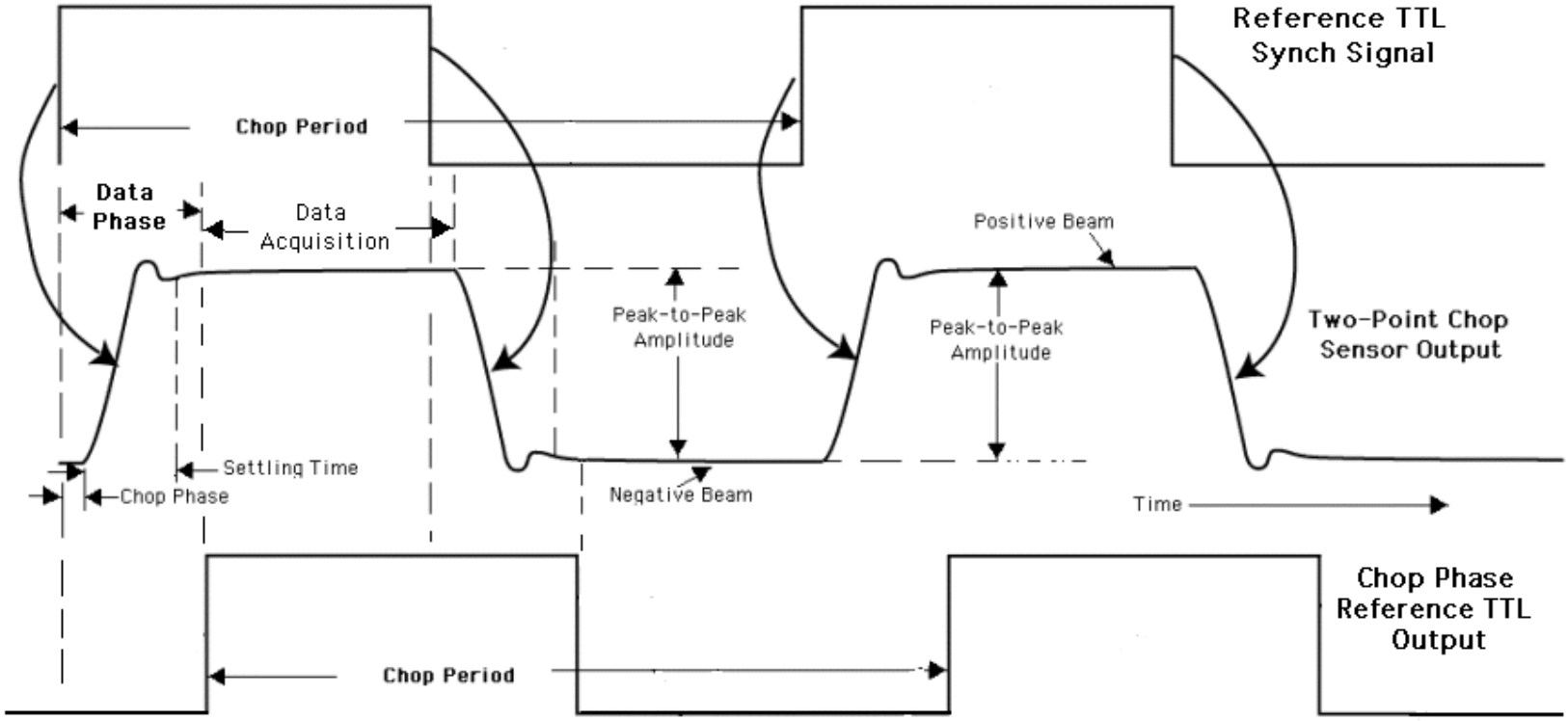
DCR-0106.R1 in regards to Chop Stability

- Requirement: Stability of chop phase angle shall be < 0.5 degree for frequencies up to 7 Hz, increasing linearly from 0.5 to 1.5 degrees for frequencies corresponding to 7 Hz to 20 Hz.

- This requirement is met for the Internal Sync and External Analog Modes

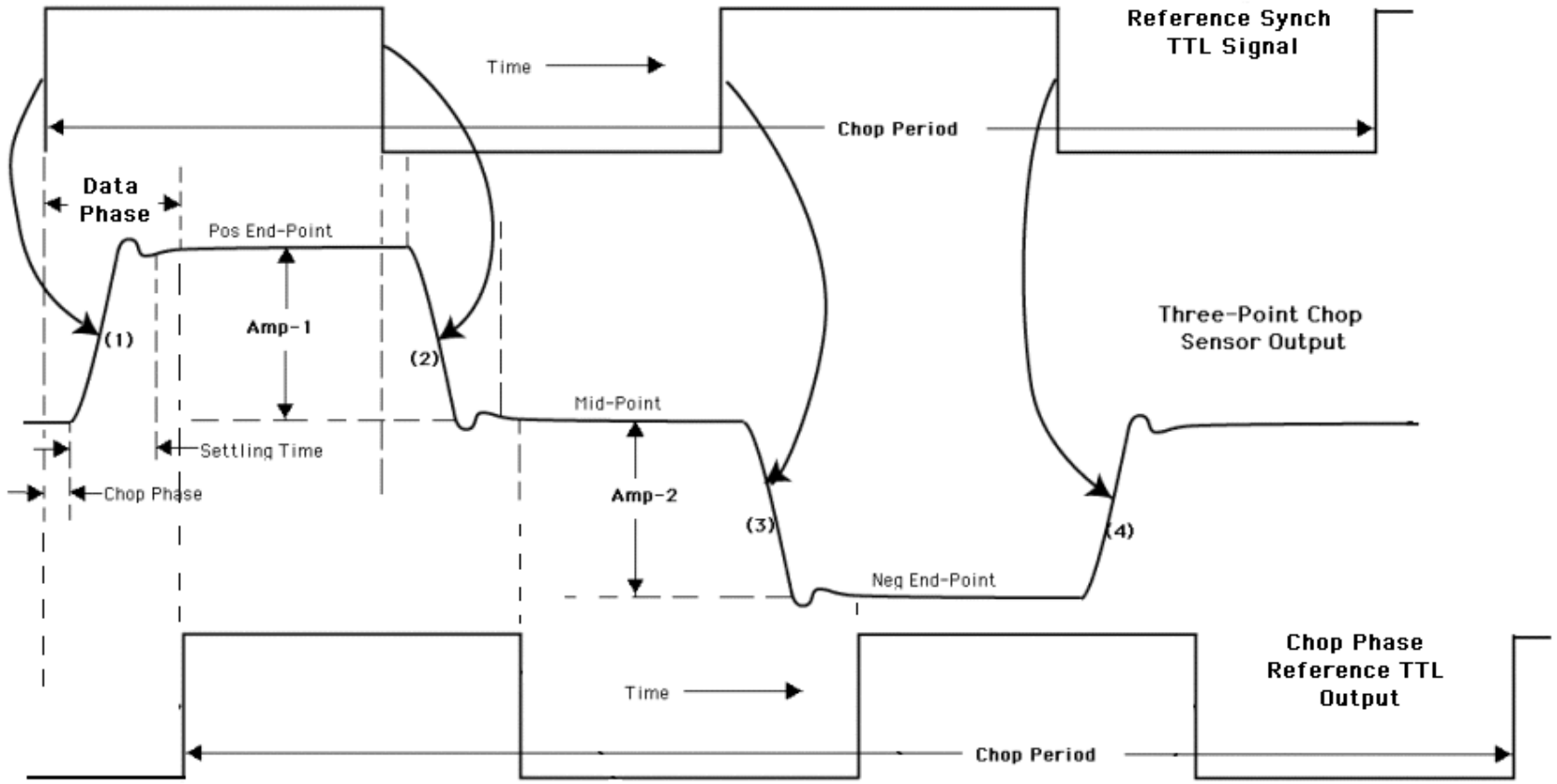
- This requirement is not met for the External TTL Sync Mode, but would if the External TTL Sync input is synchronized to the SMA clock using the 40 kHz SMA clock interface (see slide 3). With such synchronization, will have the same phase stability as for the Internal Sync Mode.

Chop Phase Reference TTL Output for 2-Point Chop



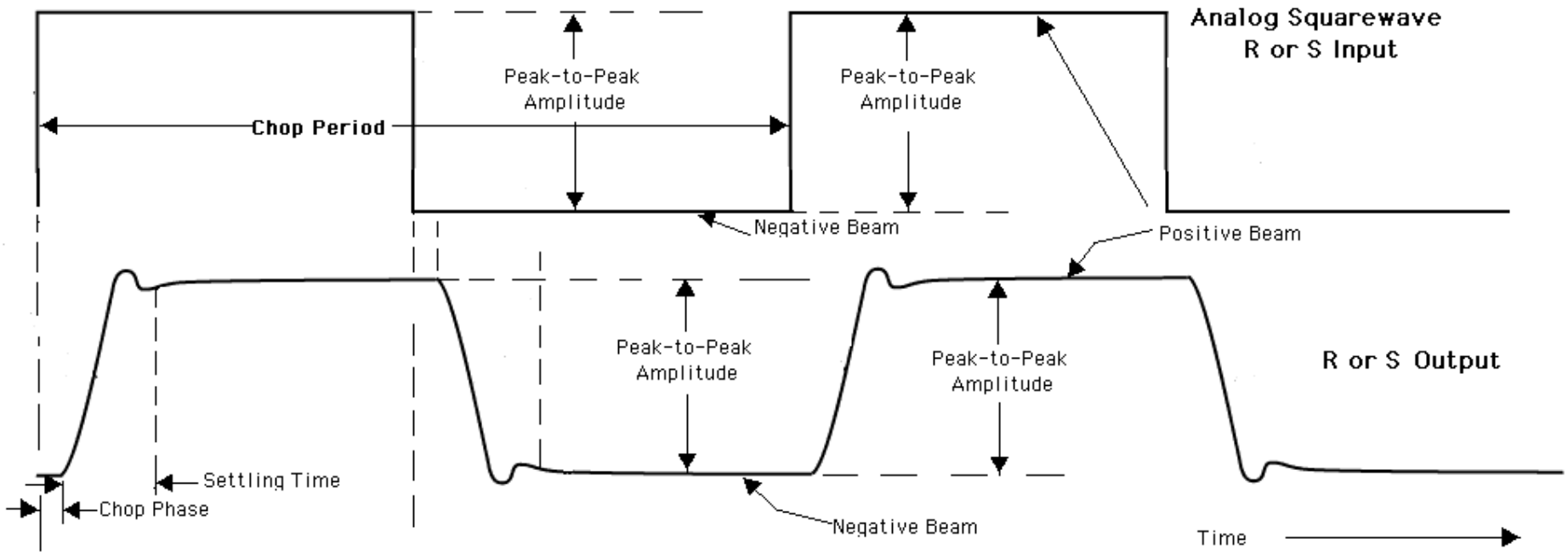
Chop Phase Ref TTL Output corresponds to Ref TTL Output but with a phase lag equal to the “Data Phase” as determined by the PI and entered using the MCS command TCM_DES_PHASE.

Chop Phase Reference TTL Output for 3-Point Chop

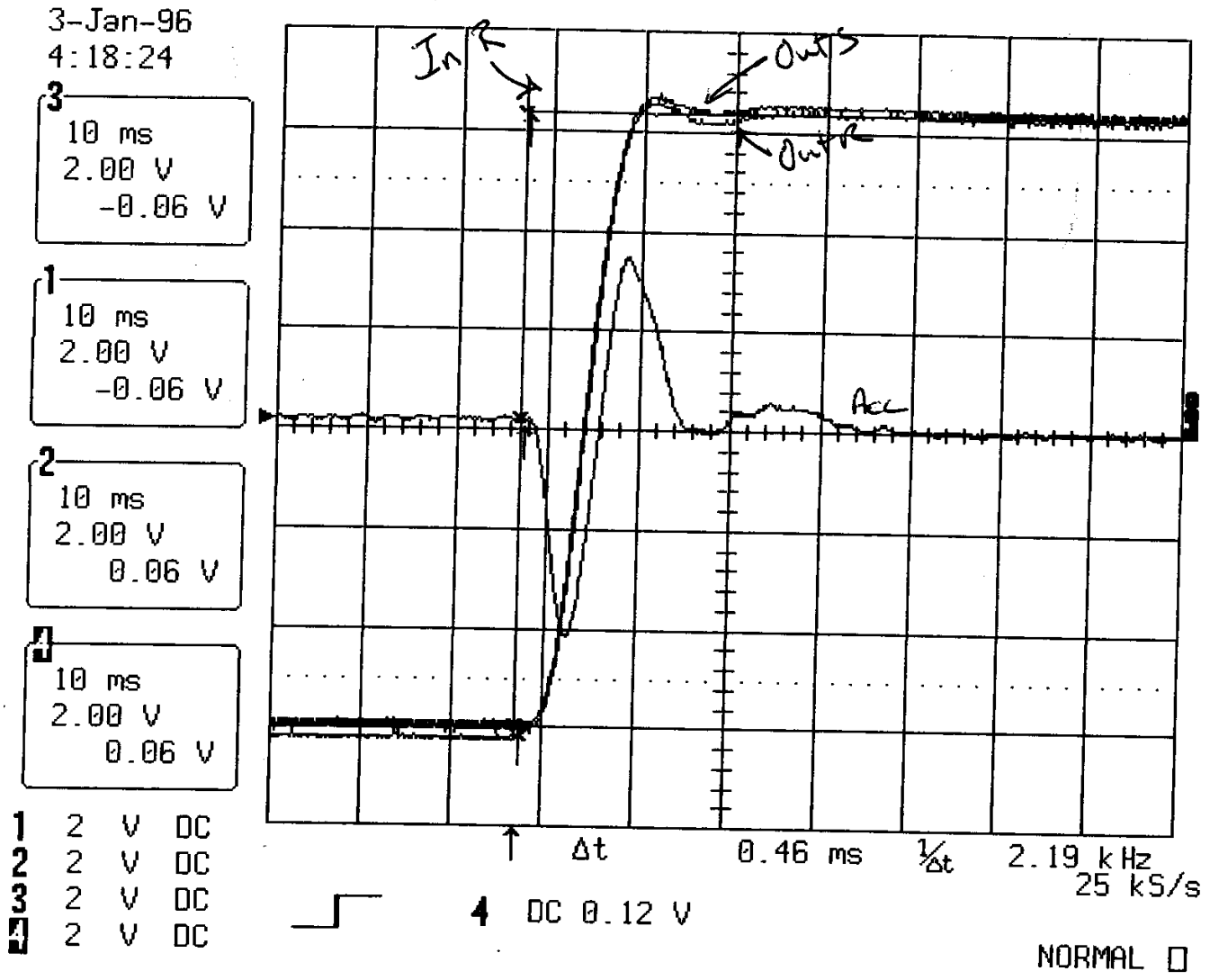


Chop Phase Ref TTL Output corresponds to Ref TTL Output but with a phase lag equal to the “Data Phase” as determined by the PI and entered using the MCS command TCM_DES_PHASE.

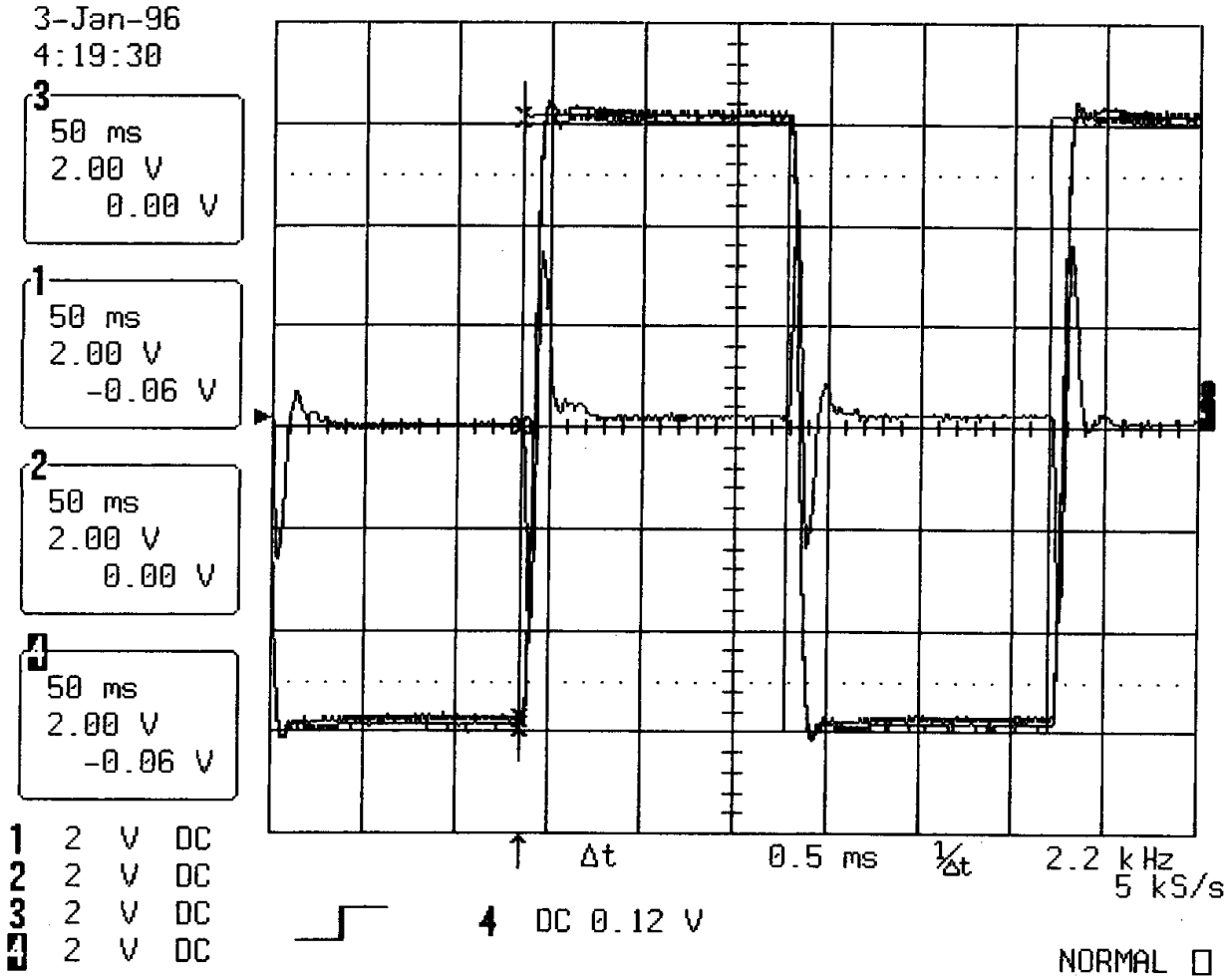
External Analog Square Wave Chop



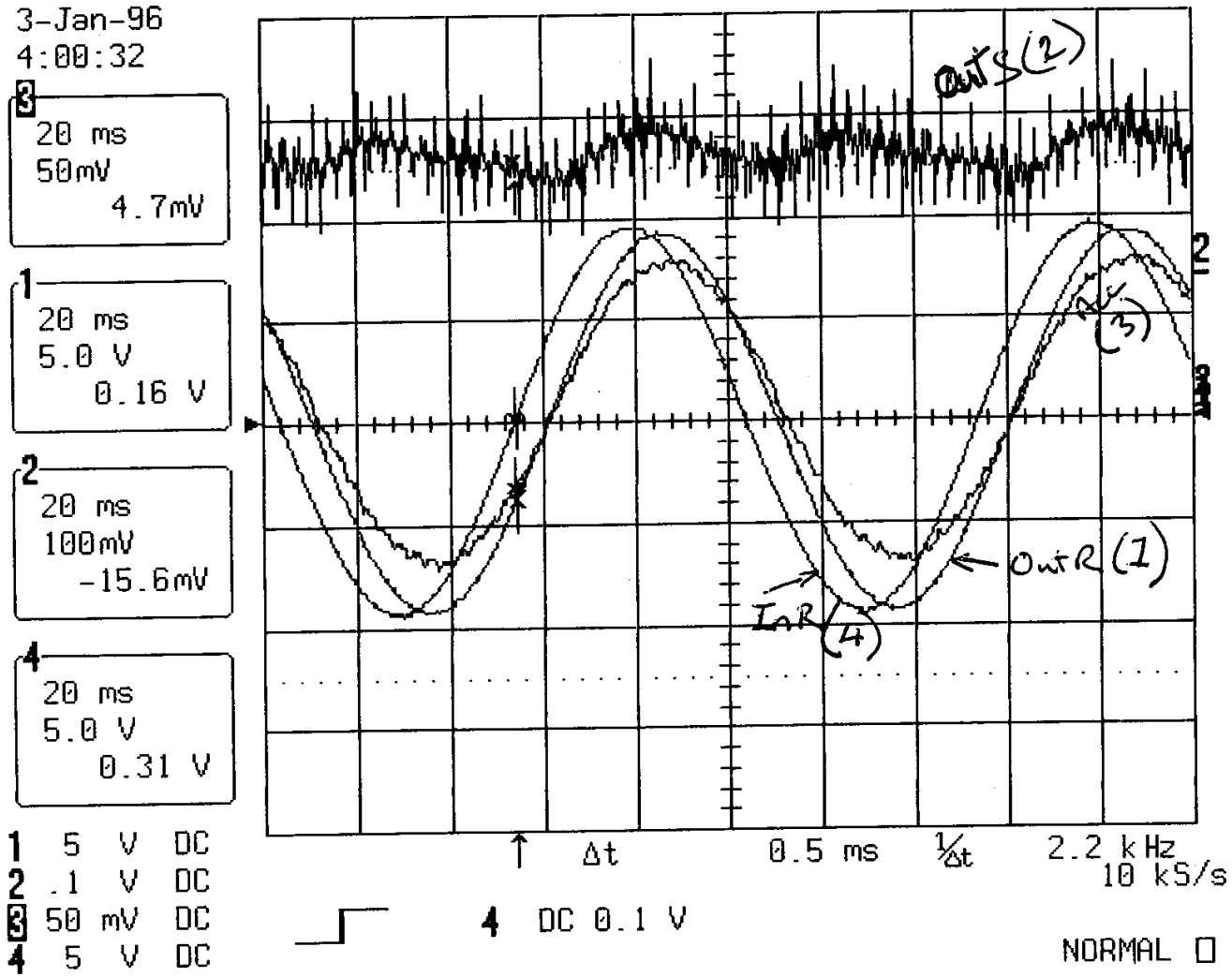
Actual 3.5 Hz external analog chop waveform with Amplitude = 9.7 arcmin at Chop Angle= 45 deg



Same as previous page but with more cycles



Actual 10 Hz external analog sinusoidal chop waveform with Amplitude = 10 arcmin

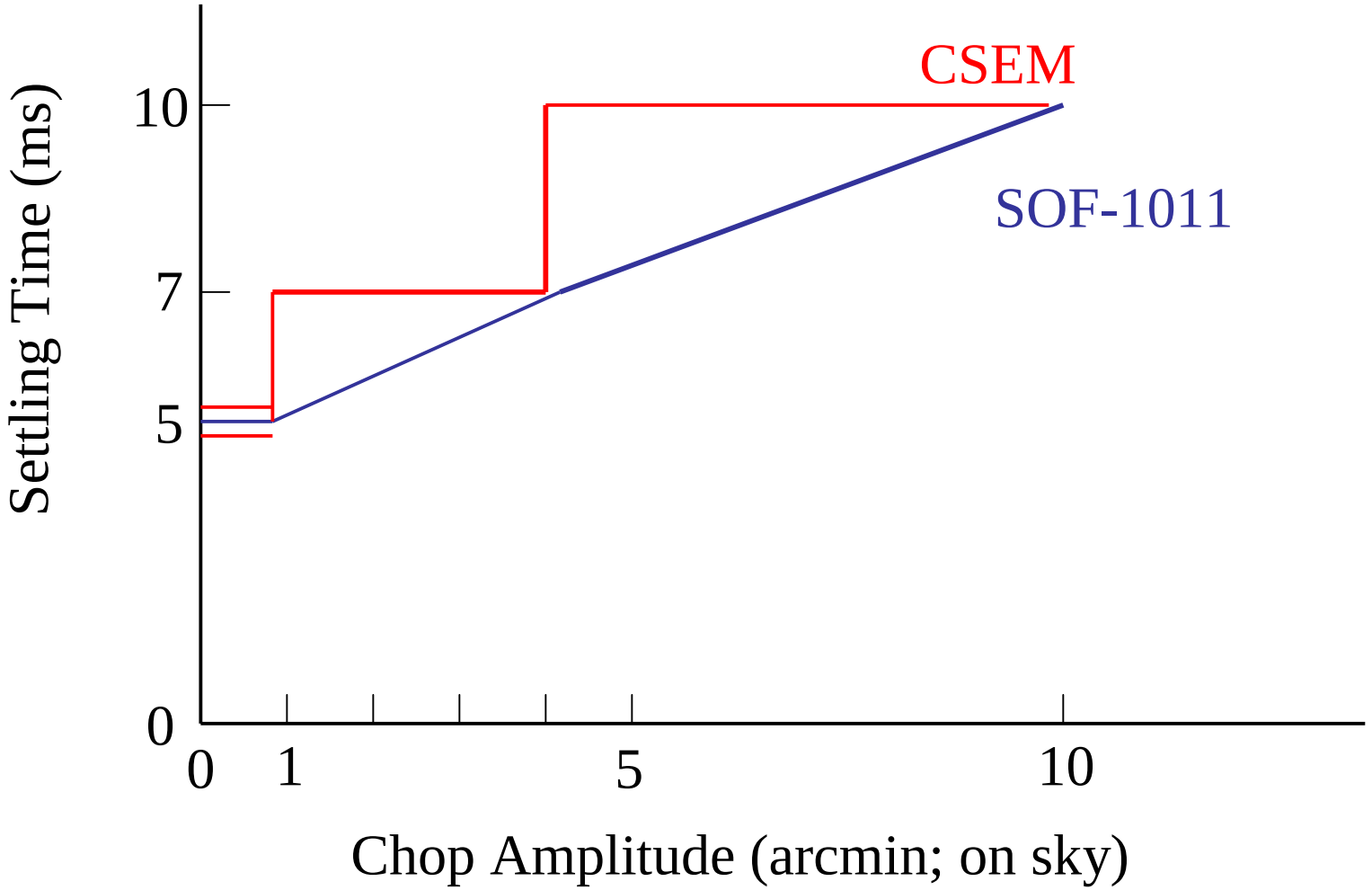


Note:
Curve 3 is the output of an accelerometer on the dummy mirror. This is almost in phase with the R analog output, implying little time lag between mirror motion and the analog output signals

Summary Comments on SMM Tests at CSEM: TCM

- TCM basically works with some exceptions.
  - Exceptions to be corrected by CSEM and tested June 24th - July 12th.
- TCM can be tuned for real Secondary Mirror (shown by demonstration) - most tests done with dummy mirror
- TCM currently doesn't meet all settling time requirements - but is close
  - After CSEM software additions (i.e., feed forward techniques), will approximately meet settling time requirement for External and Internal TTL modes (see slide 22)
  - SMM will have ~ 10 ms settling time for analog modes
- Request CSEM to test TCM over more chopper phase space
  - CSEM will carry out internal testing covering more chop angles and chop offsets
- Awaiting data to be analyzed by CSEM in regards to chop stability, but from the oscilloscope plots looks stable over an hour period (see following page 23)
- Tip/tilt of SM within 10% of commanded tip/tilt
  - Linear within 10%

Settling Time versus Chop Amplitude

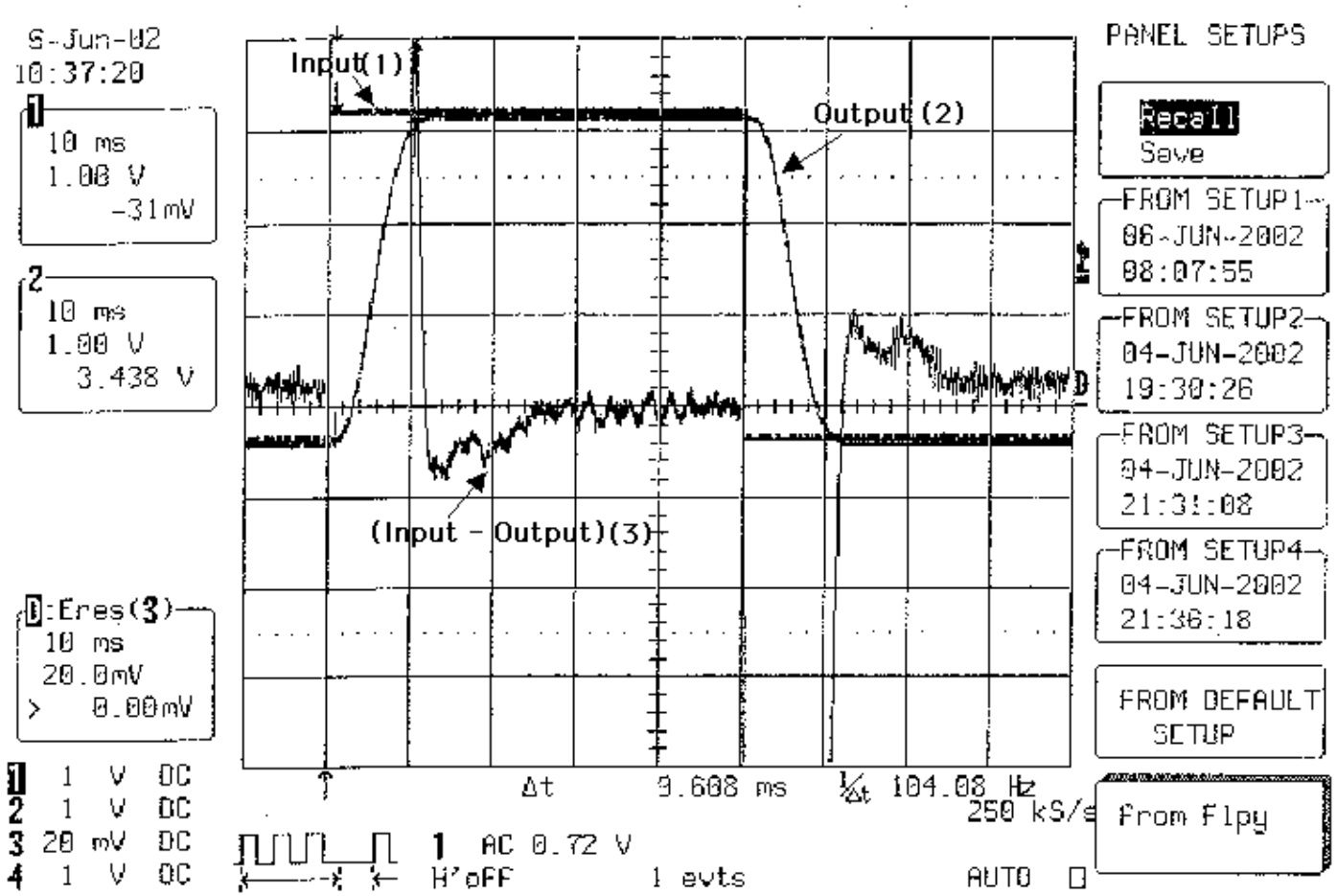


1 hour stability of ±1.6 arcmin, 10 Hz internal chop:

Plots at 0 min, 15 min, 30 min, 60 min the same

-> Phase stability < 0.5 ms (1.8 deg) meas. limit; DCR0106 -> 0.7 deg

-> End-point stability < 0.5% within spec



FCM (Focus Centering Mechanism) and Future Tests

- FCM could not meet all offset range requirements
  - Will be correct by CSEM and tested June 24th - July 12th
- **A concern**: Resonances occur when FCM moved to some offset positions while TCM chopping
  - CSEM to investigate and correct
  - Concern FCM is not stiff enough
  - May be the connection to the test marble table, however
- SMM will be tested in Augsburg late July on the spider vanes at 40 deg elevation (with dummy mirror)
- SMM will be tested in a cold environment (-60 deg C) in July or August (with dummy mirror)

Conclusion of Telecon Discussions with SI Teams

- SI Teams accept CSEM provided settling times (slide 22)
- (SI Teams yet to respond to chop stability measurements - came in after the telecon. However, the phase stability as measured looks acceptable.)
- SI Teams in general pleased with the chopper performance (i.e., TCM performance) on the bench, and the SI/SMA interfaces provided.
- Pleased the SMM retuneability was demonstrated with the real Secondary Mirror.
- Concerned about possible resonance problems with the FCM in other than centered position.
- Concerned about sensitivity of SMM to different environments (i.e., attached to spider vanes in cold and “windy” environment of the cavity at different telescope elevations). SI Teams will be very interested in the results from future spider-vane and cold environment tests. How robust is the SMM tuning to different environments expected during flight operations? How will chopper performance differ from these bench test results presented once the SMA is in flight conditions?