Gilbert Cell Multiplier Measurements from 2-18.5 GHz

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1   Overview and summary

This note summarizes a set of measurements of the Gilbert Cell multipliers from 2-18.5 GHz, the nominal spectrometer band, at 10 V bias. Steve Maas designed the multipliers for fabrication with the GCS foundry InGaP/GaAs HBT technology. These transistors should have f_T and f_{max} of about 70 and 100 GHz, but Steve's preliminary analysis of results from the test amplifiers from the prototype run indicate values closer to 50 and 70 GHz. Two multiplier circuits are on the mask: MULT1, which has an postamplifier after the Gilbert cell multiplier core, and MULT2, which has the same multiplier core (?) but no postamplifier. Both circuits have provision for varying internal bias through an additional pad, so there are four sets of data: both multipliers with the additional bias line left open and at the same potential as the general chip DC bias. Although the multiplier inputs and outputs are differential, the measurements here are single-ended, with one input (or output) left open.

Measurement of the multiplier's response versus frequency show 3 dB bandwidths of about 16 GHz. MULT1 (the design with an internal postamplifier) without additional bias has the best performance: its gain is highest and its output signal to noise ratio is the most favorable. The only disadvantage to operation without additional bias is that the multiplier linearity is somewhat better with the additional bias than without.

For MULT1 with no additional bias connection, the maximum signal level for reasonably linear operation is -13 dBm. Device quiescent power dissipation is 256 mW in this mode. The output noise density is about 1 $\mu V_{rms}/\sqrt{Hz}$ at 100 kHz, with the noise power spectrum already beginning to flatten.   Taking this and the 3 dB output bandwidth of approximately 5 MHz into consideration, it seems that phase switching at frequencies of 100 kHz to a few MHz is appropriate.

A brief analysis shows that it is possible to build a spectrometer with the existing device. The input power to each device would be approximately –20 dBm at a 100 kHz phase switch, and a 1 ms integration time input provides a dynamic range of 6 to 9 dB. These requirements are straightforward to meet.

2   Setup

Figure 1 and Figure 2 are overviews of the very simple probing setup: the chips lie on flat parts of the vacuum chuck of the Suss PM5 probing station. There is a direct electrical connection between the chuck and the Agilent 8722D network analyzer's ground terminal to establish ground potential before contact and to bleed off any static on the chuck.

DC bias was through a needle probe, with ground return through the microwave probe ground contacts and cable jacket. There are no bypassing capacitors. One DVM measured the bias voltage across the device, with a second DVM in series with the bias to measure current. The power supply was a standard lab supply which was always on but set to zero volts during contact and disconnect from the multiplier chips. The multipliers have a separate "bias" pad for changing the bias current in the device. A second needle probe, connected in parallel with the main DC bias, could contact this pad. This contact was made or broken "hot" without changing the DC power supply voltage.
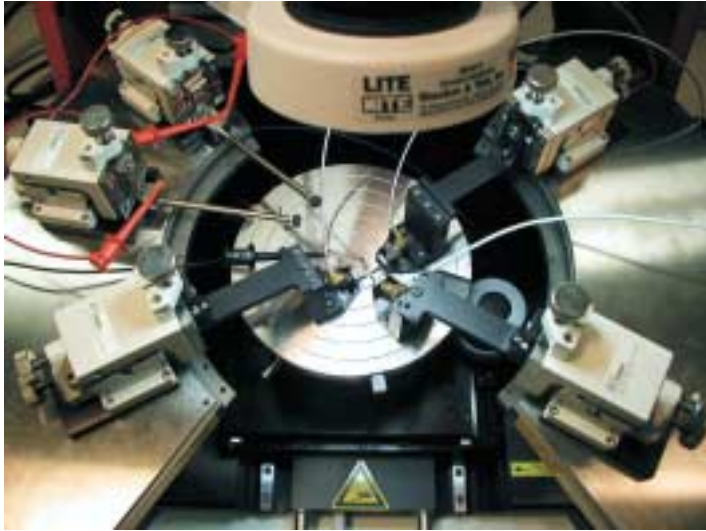

Figure 1: View of probe station and chuck showing probe and micropositioner placement
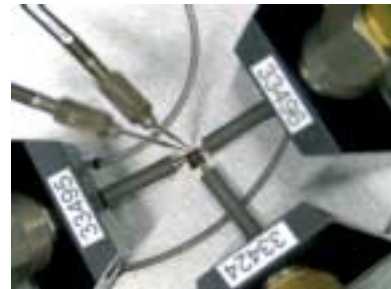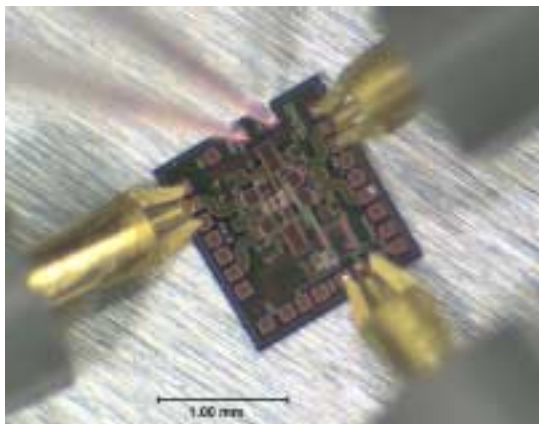

Figure 2: RF and DC probes

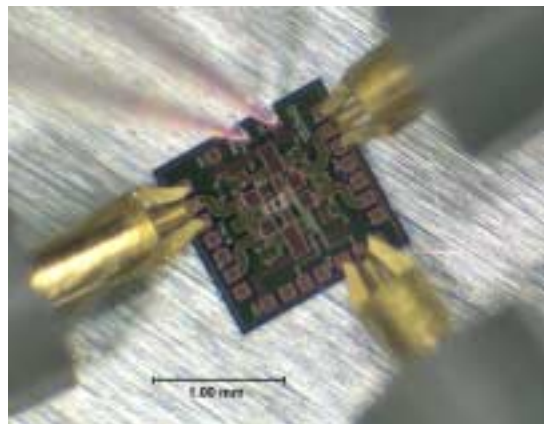Figure 3: Contacts to MULT1 chip

Figure 4: Contacts to MULT2 chip

Figure 3 and Figure 4 show the contacts to the multiplier chips. Unused inputs are open. One ground contact on the probe at the output is bent and does not contact the chip, but the other ground is good. This should not introduce any significant errors since the output frequency was 50 kHz for almost all measurements, and was always below 5 MHz.

At the multiplier inputs, separate 27.5 inch long 085 conformable cables connect each Picoprobe 40A probe to the network analyzer's test cables or to a HP 8671B frequency synthesizer. For nearly all of the measurements the 8671B fed multiplier input IN1, with port 1 of the 8722D network analyzer, in cw mode, feeding input IN2. The multiplier output could be displayed on a Tek TDS224 digital oscilloscope or on a Stanford Research Systems SRS770 low frequency (0-100 kHz) spectrum analyzer. For most measurements the synthesizer was set 50 kHz above the nominal frequency and the output was measured using the spectrum analyzer's ability to find the peak signal within its band. With an average of 200 readouts, repeatability was within a few percent. The output signal was typically 30 dB or more above the noise floor. (The noise floor was clearly due to close-in noise from one or both of the signal sources: the floor had the characteristic shape of a phase-locked source.)

The exception to this setup was for input match measurements, for which port 2 of the network analyzer was connected to multiplier input IN1. Microwave calibration was taken from the stored values in the analyzer, which were made with standard short-open-load-through measurements on a GGB CS-5 calibration substrate and the same cables and probes. Calibration includes the constants GGB supplied with the probes.

3   Measurements

3.1   DC bias

Table 1 shows the DC bias conditions for both multipliers with and without contact to the additional bias pad. M1 is MULT1; M2 is MULT2; NB indicates no additional bias; and B indicates additional bias.

	M1NB	M1B	M2NB	M2B
Voltage	10.03 V	10.02 V	10.05 V	10.04 V
Current	25.5 mA	31.0 mA	16.3 mA	21.9 mA
Power	256 mW	311 mW	164 mW	220 mW

Table 1: DC bias conditions

3.2   Response versus input frequency

Figure 5 shows that the multiplier is flat within 3 dB between 2 and 16 GHz. Data in this figure are taken at –25 dBm power on both ports with a 50 kHz beat note. The points are corrected for source output power (small corrections, measured with an HP437B power meter and Agilent 8481D power head) and cable and probe loss (measured with the 8722D network analyzer and a short section of line on the GGB SM-5 calibration substrate). Since the loss enters in voltage rather than power, the cable and probe loss is half the value measured with the network analyzer (adding a 3 dB pad to each cable would reduce the output by 3 dB but would measure out as 6 dB with the network analyzer). The output has been scaled by a constant factor for all measurements, and relative differences are correct.
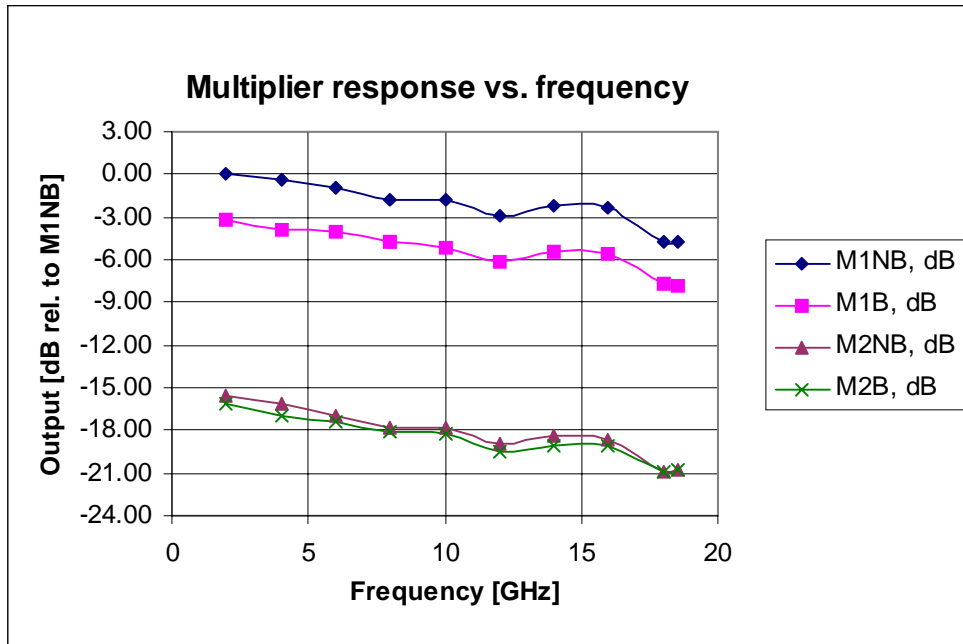
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Multiplier response vs. frequency

Figure 5: Multiplier response vs. frequency for both multipliers with and without additional bias. M1 is MULT1; M2 is MULT2; NB denotes no additional bias; and B denotes additional bias. The output scale is arbitrary but is constant for all measurements, so relative differences are correct.

Figure 5 shows that the highest responsivity setup is for MULT1 without additional bias. Adding bias does not change the band shape but reduces the gain by a uniform 3 dB. MULT2, which does not have an output amplifier stage, has about 16 dB less gain than maximum and only a small change with or without additional bias.

3.3   *Saturation*

Figure 6 shows MULT1's output saturation with equal input power levels at 5 GHz. The measurements were in pairs, with and without additional bias at each power setting before changing power, so the relative compression at each power level is unaffected by setting errors. Power levels are the nominal output levels given by the signal source front-panel settings and are corrected for cable loss.
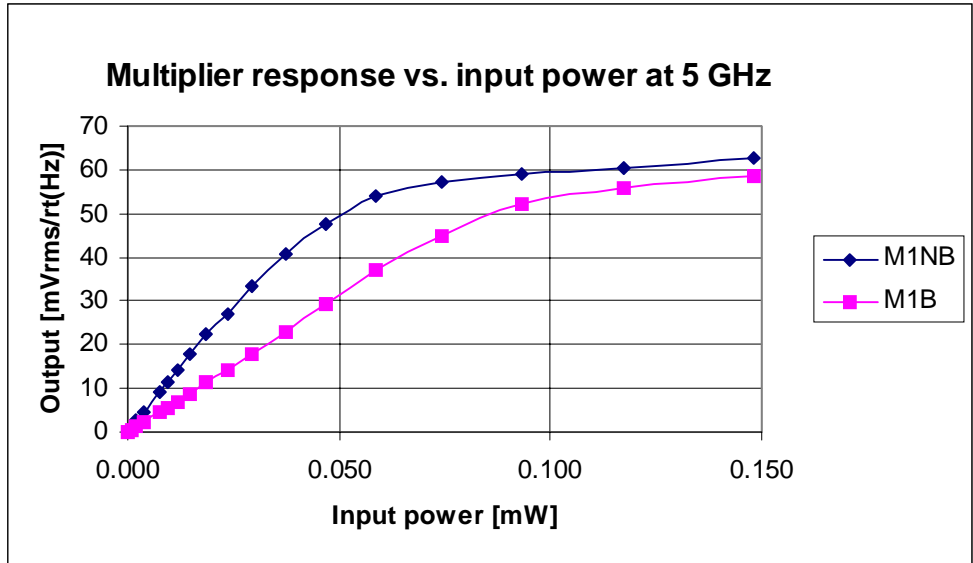
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Figure 6: Multiplier response vs. input power at 5 GHz.

Not surprisingly, the device saturates sooner without additional bias because the device gain is higher without additional bias. A useful upper limit to the input power for MULT1 is -13 dBm, or 0.05 mW. Saturation is gradual to about 3.1 V pk-pk at the output, with a noticeably distorted sine waveform, after which the saturation curve kinks and flattens considerably. Output levels at saturation are about the same in both cases. The multiplier response is more linear with additional bias, but nonlinearity can be easily modeled and corrected.

3.4   Low-frequency noise at IF

Both signal sources were switched off but the probes still in place for low-frequency noise measurements with the SRS770 spectrum analyzer. The cabling between the multiplier output probe and the oscilloscope or spectrum analyzer was a ~2 ft length of small-diameter flexible cable, then a ~1.5 ft length of RG-58. The multiplier output source impedance is low enough that rolloff from cable capacitance below 100 kHz was 1% at most, judging by substituting the short length of RG-58 for a cable approximately 7 ft long.
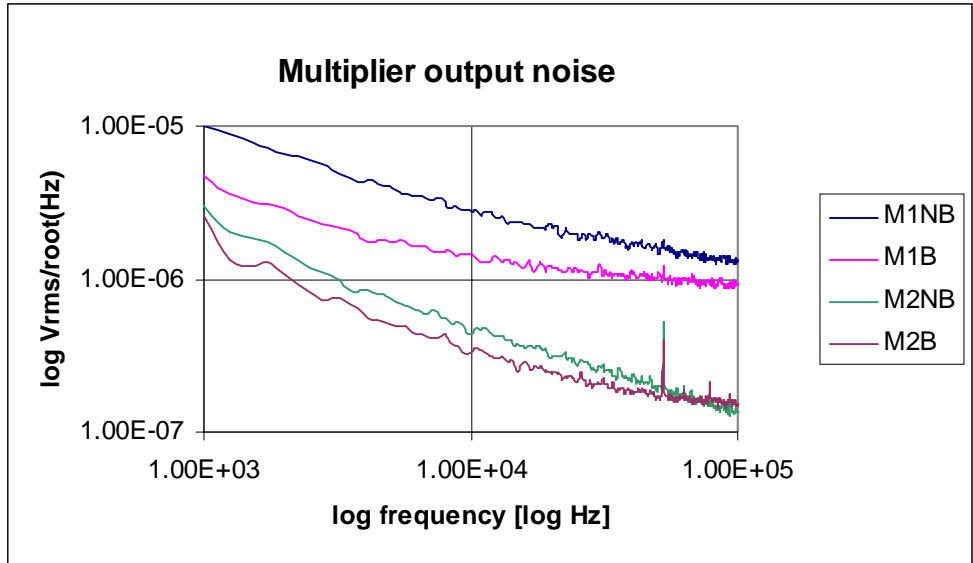
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Figure 7: Low-frequency multiplier noise for both multipliers with and without additional bias. See Figure 5 for legend key.

While the noise is higher for MULT1 than MULT2, the signal-to-noise ratio is best for MULT1 without additional bias: the responsivity is 16 dB larger but the noise is only 10 dB larger at 100 kHz. This is slightly curious since this indicates that the postamplifier in MULT1 to some extent suppresses the noise from the multiplier core. Except for MULT2 without additional bias, the noise spectra are beginning to flatten by 100 kHz, so switching at much higher frequencies will bring only a relatively small drop in noise, while the signal will drop because of IF output rolloff (sec. 3.5).

3.5   IF Bandwidth

Figure 8 indicates that the IF output bandwidth is at least a few megahertz. These measurements were made by setting the network analyzer oscillator to 5 GHz and increasing the offset from 5 GHz on the synthesizer while measuring the output signal with voltage cursors on the TDS224 oscilloscope. This measurement is complicated by loss and shunt capacitance in the output cable: rolloff is important for the IF response measurements since they reach 5 MHz. Substituting the long cable for the short cable used in the measurements made the output signal drop by about 3 dB at 3 MHz. Extrapolating, the actual 3 dB point is probably near 5 MHz. After the last measurement, an attempt to reduce the cable effects by terminating the cable with a 50 Ω load at the oscilloscope simply destroyed the multiplier chip.
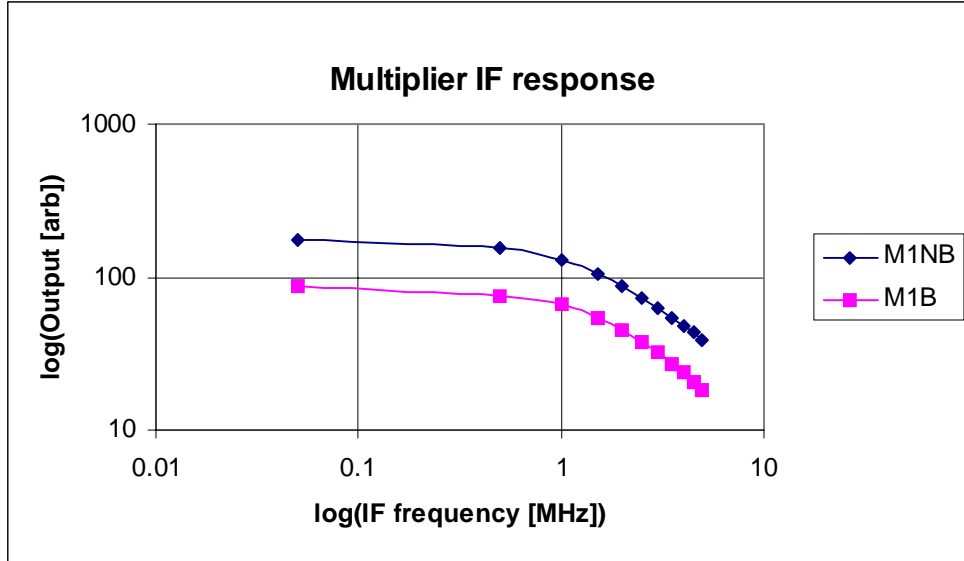
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Figure 8: Lower limit to IF response vs. IF frequency for MULT1, measured at 5 GHz. Uncorrected cable rolloff is important in this plot, and the actual IF 3 dB frequency is probably around 5 MHz.

3.6   Input match

Figure 9 shows the return loss from the multiplier inputs. The match is essentially perfect at low frequencies, with the reflections increasing slowly with frequency. These data are for MULT1 without additional bias, but the change with additional bias or to MULT2 is so small that the data in Figure 9 are quite representative for all cases.
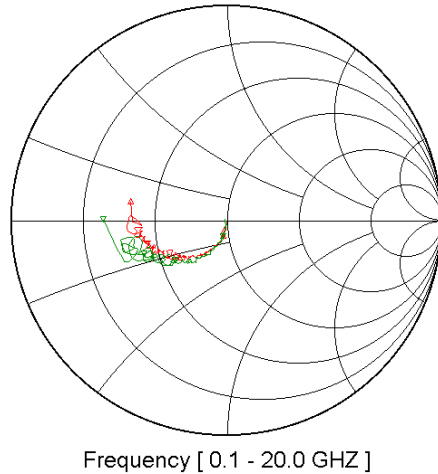

Frequency [0.1 - 20.0 GHZ]

Figure 9: Input match for MULT1 with no additional bias: green (outer curve) is S_{11} for IN1 and red (inner curve) is S_{11} for IN2.

3.7   Responsivity

Multiplier responsivity in V/mW was measured with both inputs at -25 dBm at a frequency of 5 GHz with the oscilloscope on the multiplier output. For MULT1, without

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and with additional bias, the outputs were 226 mV pk-pk (3.60 mV$_{rms}$/√Hz) and 173 mV pk-pk (2.83 mV$_{rms}$/√Hz). Table 2 is a summary of multiplier responsivities starting with the -25 dBm signal levels, taking half the peak-peak voltage since the phase runs between ±180º.

MULT1NB	MULT1B	MUL2NB	MULT2B
48 V/mW	37 V/mW	1 V/mW	1 V/mW

Table 2: Multiplier responsivities

4 Correlator properties

With noise and responsivity in hand it is possible to work out limits for correlator performance. Here we start with the necessary input power level to overcome the multiplier noise. Averaged over some integration time, the rms electronic noise from the multiplier is

$$V_{rms} = S_V \sqrt{\frac{1}{\tau}} \quad , \tag{1}$$

where S_V is the voltage spectral density in units of V$_{rms}$/√Hz and τ is the integration time in seconds.

Noise from the front end should dominate the system noise. In terms of front- and back-end variances σ_{fe} and σ_{be} the observing time efficiency η is

$$\eta = \frac{\sigma_{fe}^2}{\sigma_{fe}^2 + \sigma_{be}^2} \quad , \tag{2}$$

 or

$$\frac{\sigma_{fe}}{\sigma_{be}} = \sqrt{\frac{\eta}{1-\eta}} \quad . \tag{3}$$

To keep η above 90% (spectral *S/N* degradation of 5%) the rms noise from the front end should be at least a factor of three larger than the backend noise.

The radiometer equation relates the front-end noise fluctuations to the mean signal level; combining this with the factor of three from eq. (3) and the back-end noise from eq. (1) gives

$$\overline{V} = \Delta V_{rms} \sqrt{B\tau} = 3S_V \sqrt{B} \quad , \tag{4}$$

for the mean front-end signal level, with *B* equal to the input bandwidth. Converting to input power with the device responsivity *R* (units V/W),

$$P_{in} = \frac{\overline{V}}{R} = \frac{3S_V \sqrt{B}}{R} \quad . \tag{5}$$

Taking representative values for MULT1 with a phase switch frequency of 100 kHz (noise 1.3 μV$_{rms}$/√Hz), input bandwidth 16 GHz, and responsivity 48 V/mV, eq. (5) yields an input power of 10 μW, or −20 dBm. This is reasonable both in terms of device saturation and driver amplifier output power levels.

Dynamic range in the analog-to-digital converter sets the integration time. For an ADC with n bits, the radiometer equation shows

$$\frac{\overline{V}}{\Delta V_{rms}} = \sqrt{B\tau} = 2^{n-1} \quad , \tag{6}$$

with the factor of two taken in the exponent on the far right insures adequate noise sampling by the digitizer: the least significant bit size should be somewhat smaller than the rms noise level. Solving for integration time τ,

$$\tau = \frac{1}{4B} 2^{2n} \quad . \tag{7}$$

For MULT1 and a 16-bit ADC, this corresponds to 67 ms. It is easy to integrate for shorter times, and doing so adds dynamic range for input power. Solving eq. (6) for n gives

$$n = \frac{\log(B\tau)}{2\log 2} + 1 \quad . \tag{8}$$

For a 1 ms integration time, eq. (8) shows that a 13 bits is sufficient, leaving 3 bits (factor 8 or 9 dB) available for input power changes if the ADC has 16 bits.

Taken together, this means that it is straightforward to use electronics similar to WASP2's for a new correlator: analog demodulation is necessary for a 100 kHz phase switch, and reading out and accumulating the ADC data within a 1 ms integration time is easy. A faster phase switch would reduce the input power requirement by perhaps 3 dB, but switching in the MHz range would require a RF mixer rather than a simple solid-state switch. An RF mixer is larger than a switch and would require more power, but it is still a reasonable option.