High Resolving Power and Highly Compact Arrayed Waveguide Grating with Reusable Delay Lines (RDL-AWG)

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***Abstract*— Arrayed waveguide grating with reusable delay lines (RDL-AWGs) with a resolving power of 28,000 is experimentally demonstrated. The device is roughly 70 times more compact than the traditional AWG, which reduces the phase errors caused by uniformity and improves the performance of the spectrometer.**

***Keywords*— astrophotonics, arrayed waveguide grating, silicon photonics, photonics integrated circuits**

I. Introduction

Astrophotonics is an emerging field that brings the advantages of photonic integrated circuits (PICs) to astronomy applications. The on-chip spectrographs are one of the various applications that are compatible with mature CMOS processes and have been widely studied. Among various implementations of photonic spectrographs, both photonic echelle gratings (PEGs) and arrayed waveguide gratings (AWGs) are well-known technologies that have been demonstrated with good performances in terms of throughput, spectral resolving power, etc. AWGs have attracted more attention since they are relatively simpler in design and easier in fabrication.

In a traditional AWG, the arrayed waveguides are constructed to introduce a constant path difference between adjacent waveguides[1], [2]. The longest waveguide in the arrayed waveguides is at least $\lambda \cdot R$, where λ is the operating wavelength and R $(\lambda/\Delta\lambda)$ is the resolving power. As the resolving power increases, the footprint of the traditional AWG design increases monotonically, which leads to optical phase errors that are generated by fabrication imperfections [3], [4]. These phase errors degrade the performance of the device by reducing the resolving power, increasing insertion loss and cross-talk [5]. Various approaches have been studied to reduce the impact of phase-error issues, including footprint reduction and active phase compensation [6]. The footprint reduction is typically achieved by overlapping the two free propagation regions (FPRs) or adding reflectors to the ends of the arrayed waveguides. Either way could only reduce the footprint by a maximum factor of 2. Incorporating a phase shifter into every waveguide of the device would significantly increase the size, weight, power consumption, and cost (Swap-C) of the device. It also brings complexity to the chip fabrication and the testing of the AWGs.

To break the limitation in achieving high resolving power, an innovative AWG with reusable delay lines (RDL-AWG) is designed with a much more compact footprint, see Fig. 1. While traditional AWGs achieve the phase distribution using an 'array of waveguides' between the two FPRs, RDL-AWGs effectively use only a 'single waveguide' and an array of embedded direction couplers (DCs) to introduce accurate power and phase distribution to illuminate the output FPR. In this paper, we demonstrate a device with its footprint reduced roughly by a factor of 70 (and potentially more). It eliminates the need for making large AWGs and the associated step of actively compensating the phase error.

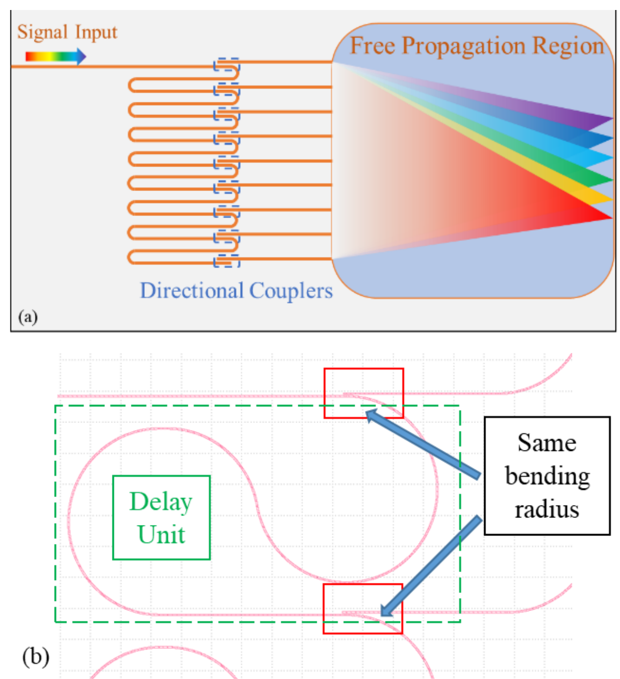

Fig. 1. (a) A schematic of the arrayed waveguide grating with reusable delay lines (RDL-AWG). (b) Delay line coupling region and delay unit.

II. Device Design

The design rules of the RDL-AWG and the embedded array of DCs has been discussed in detail in [7], [8]. The optical path length of delay line, and the coupling gap width and coupling length of DC array is carefully optimized to match the desired power and phase distributions. Especially in the coupling region, identical coupling geometry, where the bend waveguides have the same bending radius (Fig.1. (b)), is applied to ensure the accuracy of power and phase implementation. Unlike the traditional AWGs, the RDL-AWG architecture offers an easy way to achieve non-standard power distribution (or illumination) by simply optimizing each DC separately to couple a precise fraction of power in the outgoing waveguide.

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The delay line is treated as a separate design unit between adjacent DCs and is described as the delay unit in Fig. 1. (b). The delay unit is flexible in terms of the optical path length, and has fixed locations of input and output ports, which makes the RDL-AWG easy to scale to higher resolving power (with longer delay units), to wider bandwidth and more output channels (with larger number of DCs).

III. EXPERIMENTAL RESULTS

Based on the above discussion, we have designed, fabricated, and characterized one RDL-AWG device. The device is fabricated on an ultra-low loss Si_3N_4/SiO_2 on a silicon platform [9]. The structure used in this paper has layers of 10-um thermal SiO_2 as the bottom cladding, 300-nm Si_3N_4 deposited by low pressure chemical vapor deposition (LPCVD) as the core layer, and 3-um SiO_2 deposited by plasma enhanced chemical vapor deposition (PECVD) as the top cladding. The thickness of the Si_3N_4 film is chosen to be 300 nm to allow a minimum radius of curvature of 60 um while minimizing the bending loss. The RDL-AWG design was patterned using a 100 keV Elionix ELS-G100 e-beam system. The etching process is carefully calibrated to achieve the expected power and phase distribution to the output FPR, since the performance of DCs is highly sensitive to the etching depth and quality. The footprint of the device is reduced roughly by a factor of 70 compared to the traditional AWG with the same number of arrayed waveguides and grating orders, and with the same thickness of Si_3N_4.

The experimental data are shown in Fig. 2. The measured resolving power is 28,000 with a crosstalk of 16 dB, and a FSR of 0.8 nm. The on-chip peak throughput is around -4.2 dB. With the capability to fabricate the device in a compact area (0.9 × 2.9 mm^2) and with ultra-low-loss waveguide (<0.02 dB/cm) [10], we achieve a resolving power that is in good agreement with the theoretical value, which is 30,000.

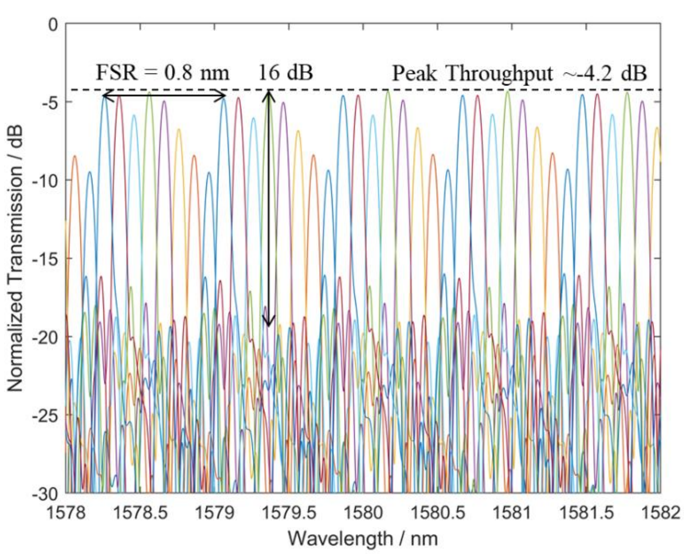

Fig. 2. Experimental normalized transmission spectrum at the output channels of the RDL-AWG.

The presented preliminary RDL-AWG has only 20 arrayed waveguides and 8 output channels. The experimental results prove that the concept to reuse the delay line to reduce the footprint works well. The next step is to build an RDL-AWG with a larger number of arrayed waveguides and output channels, which means a higher FSR. With the concept of the delay unit, it is easy to scale up the design.

The relative uneven transmission levels at different output channels are due to the power distribution difference between the simulated result and real device. A characterization of the accurate power distribution will be performed to further improve the performance.

IV. CONCLUSION

An innovative design of AWGs with reusable delay lines (RDL-AWGs) is presented, which has several unique advantages over traditional AWGs for achieving a high resolving power. An array of directional couplers is optimized to distribute the input signal from the delay line into the output free propagation region. By making the AWGs more compact, it significantly reduces the impact of fabrication imperfections and uniformity issues which prevent traditional AWGs from achieving ultra-high resolving powers. An RDL-AWG device with measured resolving powers of 28,000 and an on-chip throughput of -4.2 dB is demonstrated; it is roughly 70 times more compact than the traditional AWG.

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