Gilbert Cell Multiplier Measurements from 2-18.5 GHz
II: Sample of Eight Multipliers

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1 Overview and summary

This note summarizes a set of measurements of eight Gilbert Cell multipliers from 2-18.5 GHz, the nominal spectrometer band, at 10 V bias. With the results from the first set of measurements (I: First Measurement) indicating the most favorable circuit and operating conditions, this note reports on scatter from a sample of eight MULT1 devices operated without additional bias.

The basic results from note I remain unchanged. The scatter in response and noise are about 1 dB each, and are correlated: it appears that postamplifier gain is the dominant source of device-to-device variation. The response versus frequency and noise are slightly different in these measurements than in the first set (lower response at 2 GHz and lower low-frequency noise). A change in grounding between the two sets of measurements is the most likely source of the change. In the first measurements the chips were tested directly on the probe station's metal chuck, which in turn had a direct low-frequency ground connection to the network analyzer's ground. For the results reported here, the chips were mounted in the bottom of a Gel-Pak container, with grounding through the probes alone. It is not surprising that the low-frequency noise changed slightly with an isolated ground, but it is slightly surprising that the microwave response changed slightly, particularly at the lowest frequency.

These new measurements also show the origin of the device's compression: the DC bias at the multiplier output is typically 8 to 9 V, limiting the undistorted output signal swing to about 2 V pk-pk. The typical maximum input signal level at both ports for reasonably linear operation is -13 dBm.

Meaningful average values for response and noise describe the devices and are useful for power level calculations since the two scale together. All devices have essentially the same requirement on input power for good system noise performance. The typical noise density is about 0.7 $\mu V_{rms}/\sqrt{Hz}$ at 50 kHz, with the noise power spectrum already flattening. Phase switching at frequencies above 30 kHz are appropriate. For a 16 GHz bandwidth spectrometer the input power to each device should be approximately –20 dBm at a 50 kHz phase switch, and a 1 ms integration time input provides a dynamic range of 6 to 9 dB. These requirements are straightforward to meet.

2 Setup

The chips lie in a modified Gel-Pak case on the vacuum chuck of the Suss PM5 probing station. Figure 1 shows the contacts to the multiplier chips. Unused inputs and outputs are open. One ground contact on the probe at the output is bent and does not contact the

chip, but the other ground is good. This should not introduce any significant errors since the output frequency was 50 kHz for almost all measurements, and was always below 5 MHz.

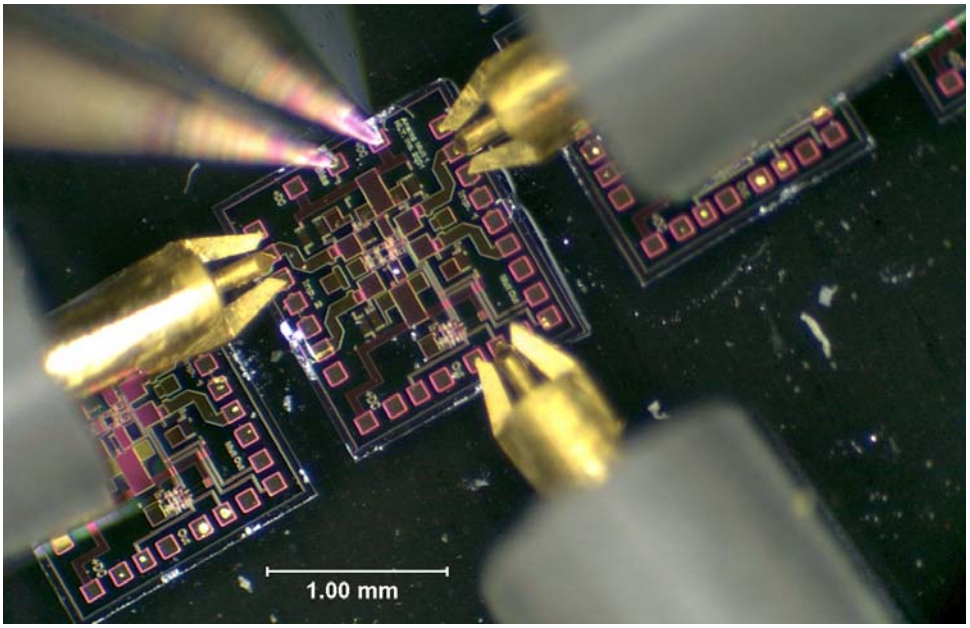

Figure 1: View of test chips with probes.

Picoprobe 40A probes contact the device inputs and outputs. At the multiplier inputs, separate 27.5 inch long 085 conformable cables connect IN2 to port 1 of an Agilent 8722D network analyzer's test cables and IN1 to a HP 8671B frequency synthesizer. The multiplier output could be displayed on a Tek TDS224 digital oscilloscope or on a Stanford Research Systems SRS770 low frequency (0-100 kHz) spectrum analyzer. For these measurements the synthesizer was set 50 kHz above the nominal frequency and the output was measured using the spectrum analyzer's ability to find the peak signal within its band. With an average of 200 readouts, repeatability was within a few percent. The output signal was typically 30 dB or more above the noise floor. (The noise floor was clearly due to close-in noise from one or both of the signal sources: the floor had the characteristic shape of a phase-locked source.)

DC bias was through a needle probe, with ground return through the microwave probe ground contacts and cable jacket. There are no bypassing capacitors. One DVM measured the bias voltage across the device, and a second DVM in series with the bias measured current. The power supply was a standard lab supply which was always on but set to zero volts during contact and disconnect from the multiplier chips

3 Results

Figure 2 and Figure 3 show normalized gain versus frequency and output noise density, averaged over eight devices in the sample. The eight chips were taken from different parts of the chip carrier supplied by GCS, so it is unlikely that they are all from the same wafer. There are some small changes compared with the results in note I: the 2 GHz

response is noticeably lower in these measurements, although the higher-frequency points are about the same, and the low-frequency noise is lower by a factor of three.

The change in low-frequency noise is not surprising since the measurement grounds are different between the first and present measurements. For the first measurements, a ground lead between the chuck and the network analyzer case provided an additional ground route compared with the current measurements on an insulating layer of Gel Pak. Eliminating the extra ground route probably improves the measurement by eliminating noise from additional sources, and the noise density of 0.7 $\mu V_{rms}/\sqrt{Hz}$ at 50 kHz is a good design number. Figure 3 shows that the noise drops rapidly to frequencies around 20 to 30 kHz, but the change with increasing frequency is slow above that. Phase switching at 30 to 50 kHz is sufficient.

Compared with the measurements in note I, the origin of the 2 GHz rolloff is still a puzzle: one would think that a change of fringing fields with the change of tests on bare chuck to Gel Pak would have a larger effect at high frequencies than at low.

The average curves for response and noise are good representations for the devices. No one device dominates in the average. Figure 4 and Figure 5 show that the shapes are generally the same within a scatter of about 1 dB.

Figure 6 shows that the output noise and response are correlated, indicating that most of the scatter comes from postamplifier gain changes. The correlation is accurate within a factor of 1.05. This is a useful result, since it means that the minimum input power, determined by a balance of output noise and input signal, is constant for all devices. Figure 7 is a plot of the minimum power as a function of frequency (the derivation of this curve is given in section 4) for a 16 GHz input bandwidth and a phase-switch frequency of 50 kHz. Input power greater than –16 dBm is sufficient for good performance in this case.

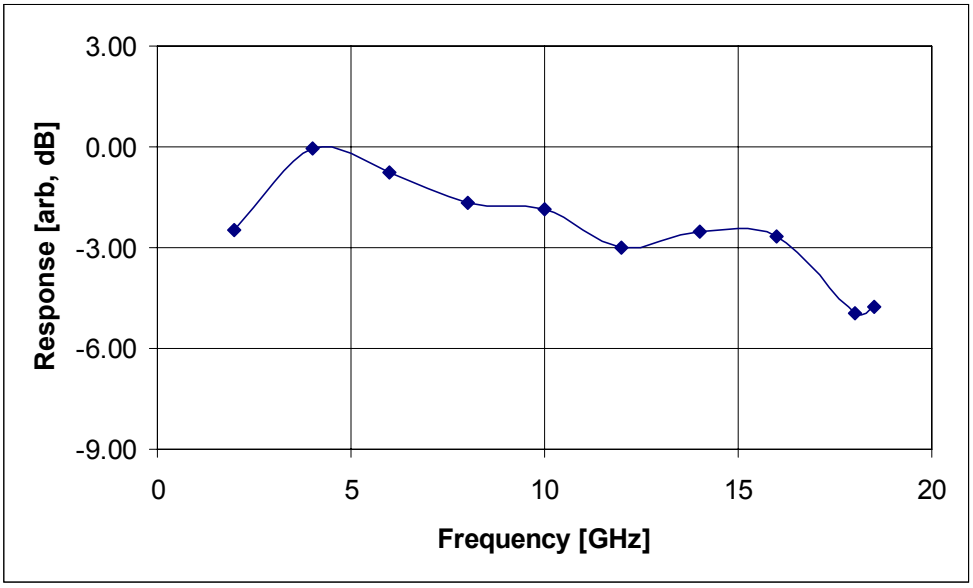

Figure 2: Average normalized response versus frequency for the sample of eight multipliers.

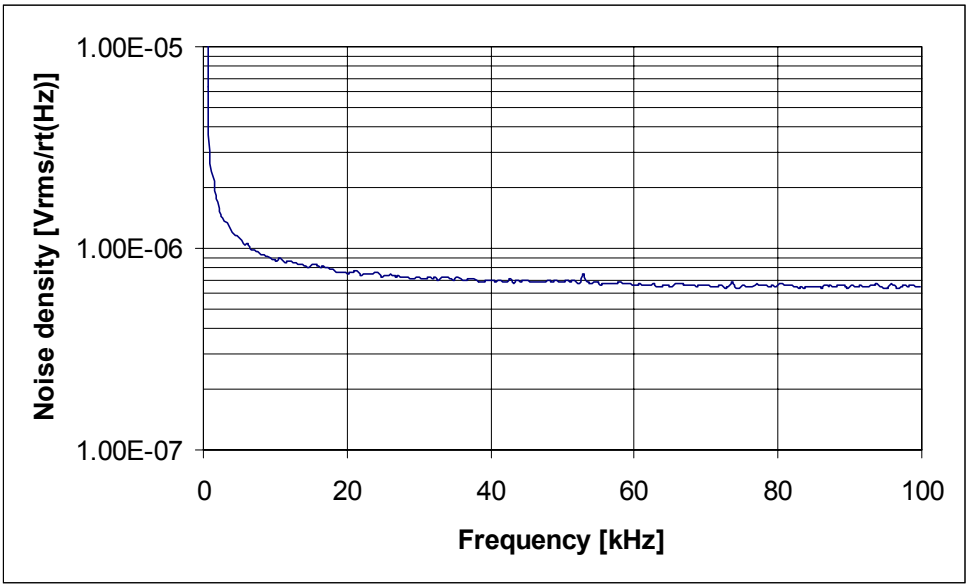

Figure 3: Average output noise versus frequency for the sample of eight multipliers.

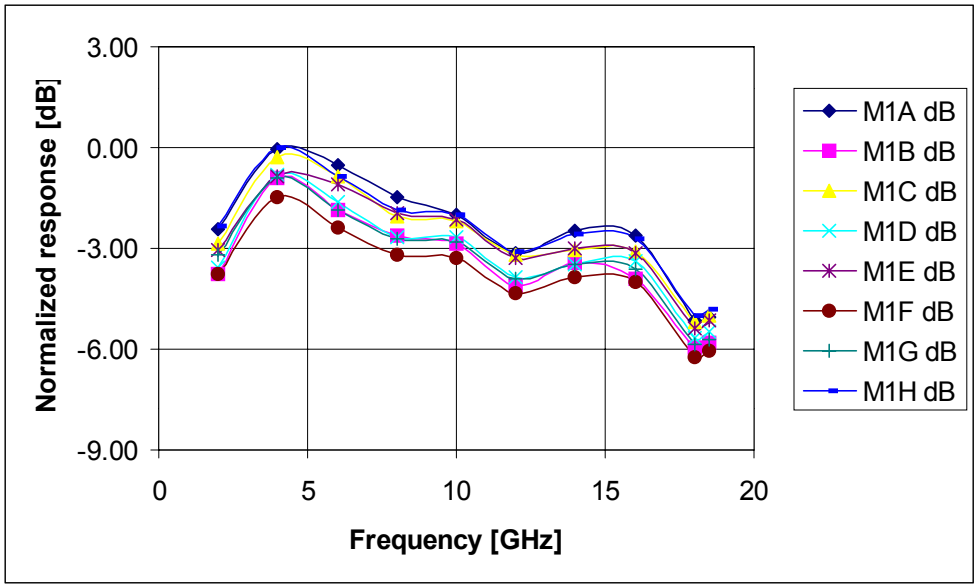

Figure 4: Response vs. frequency for a sample of eight multipliers.

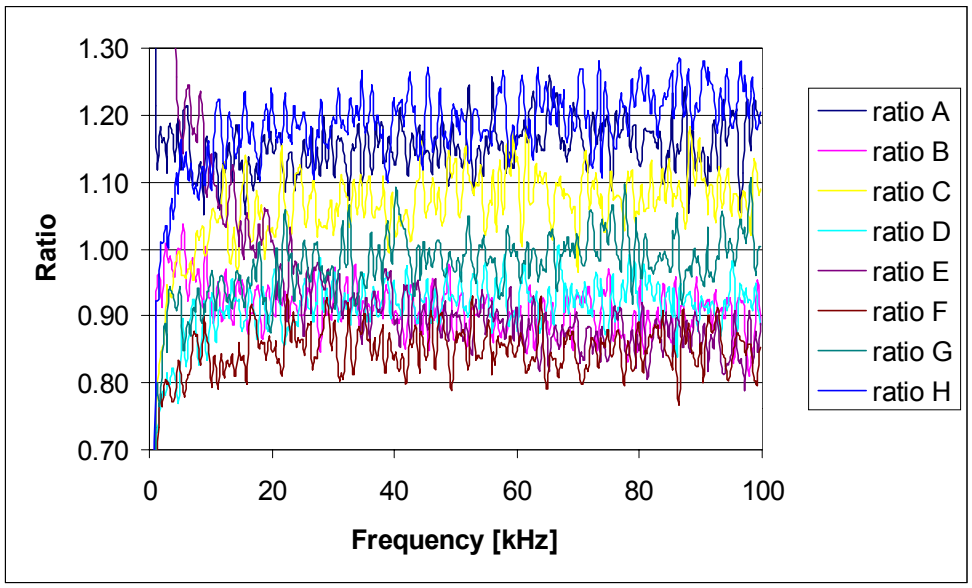

Figure 5: Noise ratio, normalized to the average, for a sample of eight multipliers.

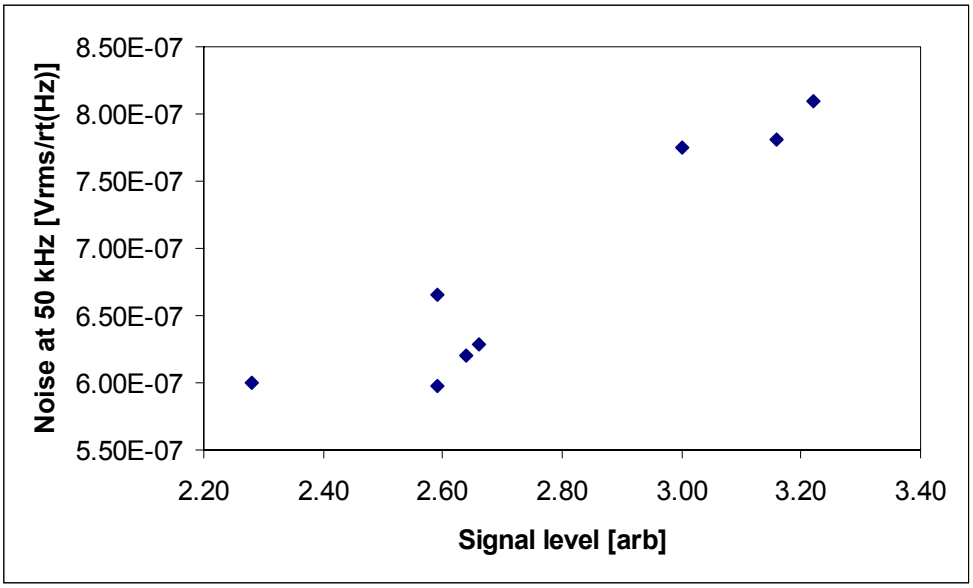

Figure 6: Correlation between output noise and responsivity for eight multipliers.

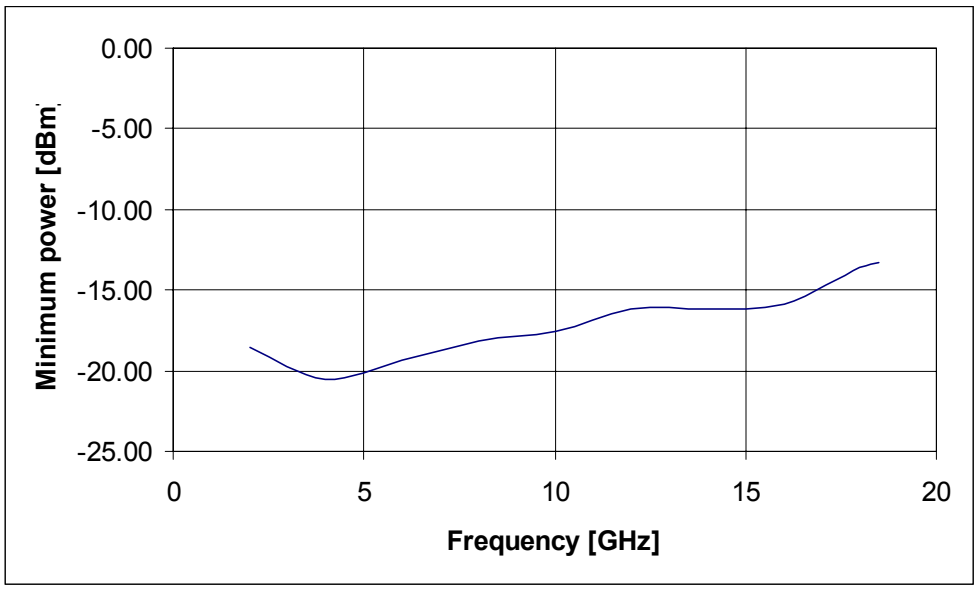

Figure 7: Minimum input power level for a 16 GHz bandwidth input.

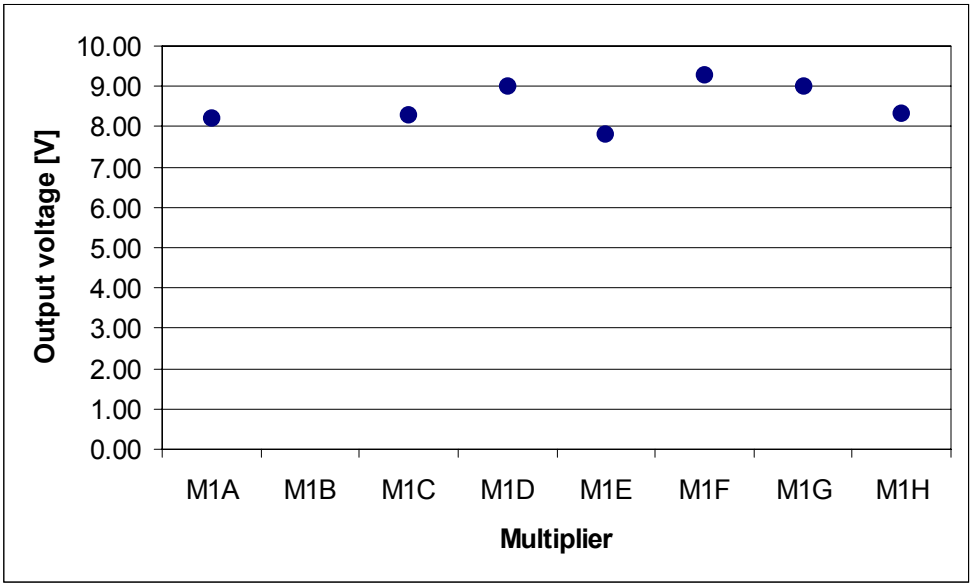

Figure 8: Quiescent output voltage for a sample of seven multipliers.

	M1A	M1B	M1C	M1D	M1E	M1F	M1G	M1H
V_{offset} [V]	8.2		8.3	9.0	7.8	9.3	9.0	8.3
I_{bias} [mA]	26.7	25.7	26.6	25.6	21.9		26.8	26.6

Table 1: Quiescent output voltages and bias currents for a sample of seven multipliers. The DC bias voltage was 10.0 V in all cases.

4 Correlator properties

With noise and responsivity in hand it is possible to work out limits for correlator performance. Here we start with the necessary input power level to overcome the multiplier noise. Averaged over some integration time, the rms electronic noise from the multiplier is

$$V_{rms} = S_V \sqrt{\frac{1}{\tau}} \quad , \tag{1}$$

where S_V is the voltage spectral density in units of $V_{rms}/\sqrt{Hz}$ and τ is the integration time in seconds.

Noise from the front end should dominate the system noise. In terms of front- and back-end variances σ_{fe} and σ_{be} the observing time efficiency η is

$$\eta = \frac{\sigma_{fe}^2}{\sigma_{fe}^2 + \sigma_{be}^2} \quad , \tag{2}$$

or

$$\frac{\sigma_{fe}}{\sigma_{be}} = \sqrt{\frac{\eta}{1-\eta}} \, . \tag{3}$$

To keep η above 90% (spectral *S/N* degradation of 5%) the rms noise from the front end should be at least a factor of three larger than the backend noise.

The radiometer equation relates the front-end noise fluctuations to the mean signal level; combining this with the factor of three from eq. (3) and the back-end noise from eq. (1) gives

$$\overline{V} = \Delta V_{rms} \sqrt{B\tau} = 3 S_V \sqrt{B} \quad , \tag{4}$$

for the mean front-end signal level, with B equal to the input bandwidth. Converting to input power with the device responsivity R (units V/W),

$$P_{in} = \frac{\overline{V}}{R} = \frac{3 S_V \sqrt{B}}{R} \quad . \tag{5}$$

Taking representative values for MULT1 with a phase switch frequency of 50 kHz (noise 700 $nV_{rms}/\sqrt{Hz}$), input bandwidth 16 GHz, and responsivity 22 V/mW, eq. (5) yields an input power of 12 μW, or –19 dBm. This is reasonable both in terms of device saturation and driver amplifier output power levels.

Dynamic range in the analog-to-digital converter sets the integration time. For an ADC with n bits, the radiometer equation shows

$$\frac{\overline{V}}{\Delta V_{rms}} = \sqrt{B\tau} = 2^{n-1} \quad , \tag{6}$$

with the factor of two taken in the exponent on the far right insures adequate noise sampling by the digitizer: the least significant bit size should be somewhat smaller than the rms noise level. Solving for integration time τ,

$$\tau = \frac{1}{4B} 2^{2n} \quad . \tag{7}$$

For MULT1 and a 16-bit ADC, this corresponds to 67 ms. It is easy to integrate for shorter times, and doing so adds dynamic range for input power. Solving eq. (6) for n gives

$$n = \frac{\log(B\tau)}{2 \log 2} + 1 \quad . \tag{8}$$

For a 1 ms integration time, eq. (8) shows that a 13 bits is sufficient, leaving 3 bits (factor 8 or 9 dB) available for input power changes if the ADC has 16 bits.

Taken together, this means that it is straightforward to use electronics similar to WASP2's for a new correlator: analog demodulation is necessary for a 50 kHz phase switch, and reading out and accumulating the ADC data within a 1 ms integration time is easy. A faster phase switch would reduce the input power requirement only modestly.