Results from the test amplifiers on the Maas prototype multiplier MMIC

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1 Test setup and calibration

Figure 1 shows the very simple probing setup for the test amplifier chips: the chips are on flat parts of the vacuum chuck of the Suss PM5 probing station. There is a direct electrical connection between the chuck and the Agilent 8722D network analyzer's ground terminal. A 27.5 inch long 085 semi-rigid flexible cable connects each Picoprobe 40A probe to the network analyzer's test cables. The network analyzer setup for calibration and measurement was stepped frequency measurements at 201 points from 0.05 to 24 GHz and output power -30 dBm.

DC bias is through a single needle probe, with ground return through the input microwave probe ground contacts and cable jacket. There are no bypassing capacitors. One DVM measured the bias voltage at the power supply, with a second DVM in series with the bias to measure current. The power supply was a standard lab supply which was always on but set to zero volts during contact and disconnect from the amplifier chips.

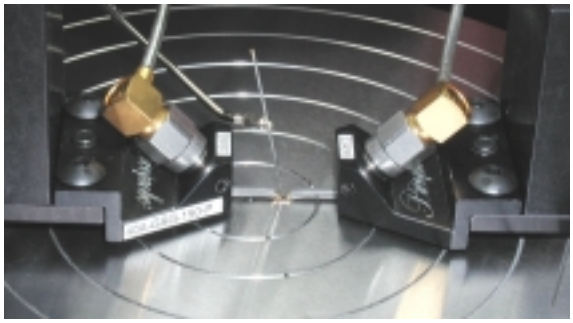


Figure 1: Test amplifier on prober chuck.

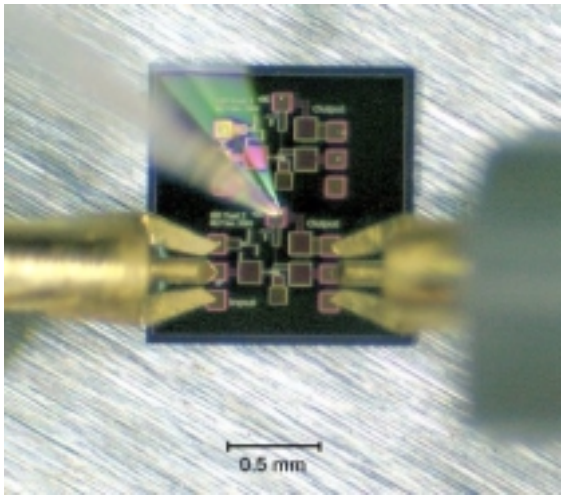


Figure 2: Probing the test amplifier.

Microwave calibration is through standard short-open-load-through measurements on a GGB CS-5 calibration substrate. Calibration includes the probe constants supplied with the probes. Tests on short lines on the substrate showed reasonable values for S_{21} and S_{12}, with deviations of 0.01 dB p-p at high frequencies. S_{11} and S_{22} also tested out well on and 25 and 100 Ω loads on the chip, with values clustered values around the nominal resistance within a couple of ohms at all frequencies. The 100 Ω load showed about 2 Ω of capacitive reactance, on average; the 25 Ω load about 1 Ω of inductive reactance.

2 Results and comparison of the three test circuits at nominal bias

Figure 3 shows the gain of the three test circuits at their nominal 10 V DC bias. Table 1 gives the bias conditions: all draw about 15 mA, slightly more current than the 12 mA expected. This is slightly puzzling since the current should be set by resistors, and the resistance specs look good. The three amplifiers have design properties:

- Test 1: Emitter feedback and 50 Ω terminations on the input.
- Test 2: Same as 1, but no 50 Ω terminations.
- Test 3: Same as 1, but no 50 Ω terminations or feedback.

Comparison of measurements and modeling for amplifier Test 1 in Figure 4 and Figure 5 shows more gain slope across the band than expected, both excess gain at low frequencies and an apparently missing gain peak near 10 GHz. This general behavior is common to all amplifiers. For further comparisons, Section 4 contains the modeling data and Section 5 contains measurements for all amplifiers with a range of bias conditions. All of the amplifiers have S_{12} < -25 dB (not shown here).

We tested two chips of Test 1 and Test 2; both chips had essentially identical characteristics. The excellent repeatability indicates an absence of probing contact problems.

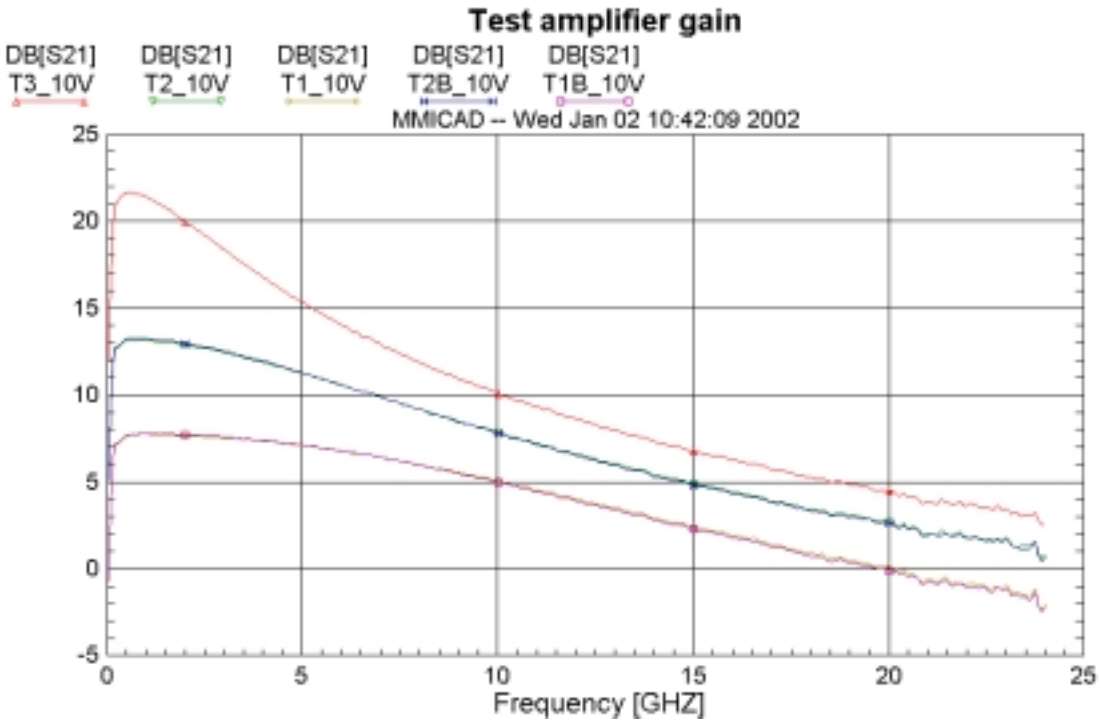


Figure 3: Forward gain of the three test amplifiers at 10 V bias. T3 is amplifier Test 3, T2 is amplifier Test 2, and T1 is amplifier Test 1. The traces from two samples of Test 1 and Test 2 amplifiers are nearly indistinguishable at the scale in this plot.

Amplifier	Bias, chip A		Bias, chip B	
Test 1	10.01 V	14.71 mA	10.07 V	15.04 mA
Test 2	10.03 V	14.65 mA	10.05 V	15.09 mA
Test 3	10.06 V	18.12 mA		

Table 1: Bias conditions for the amplifier tests of Figure 3

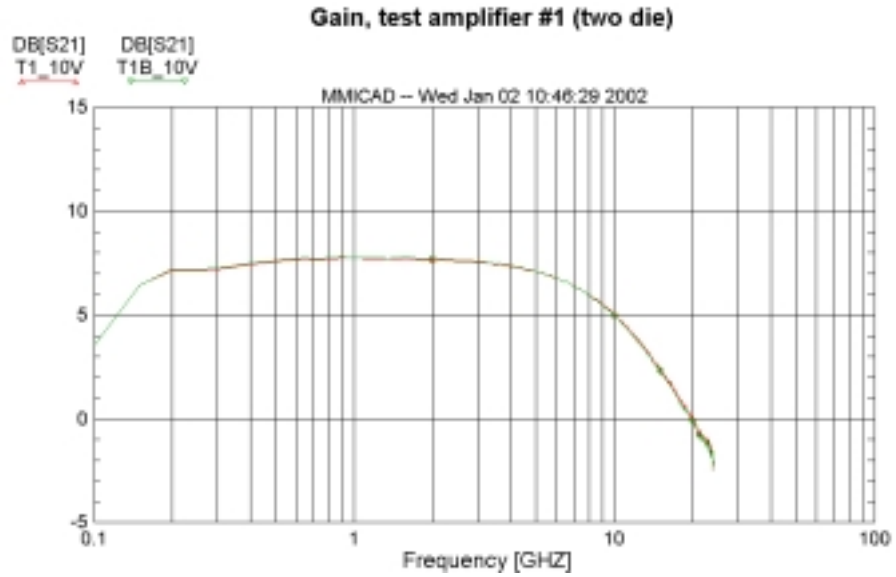


Figure 4: Data from two die of amplifier Test 1 on a logarithmic frequency scale for comparison with the modeled gain (Figure 5).

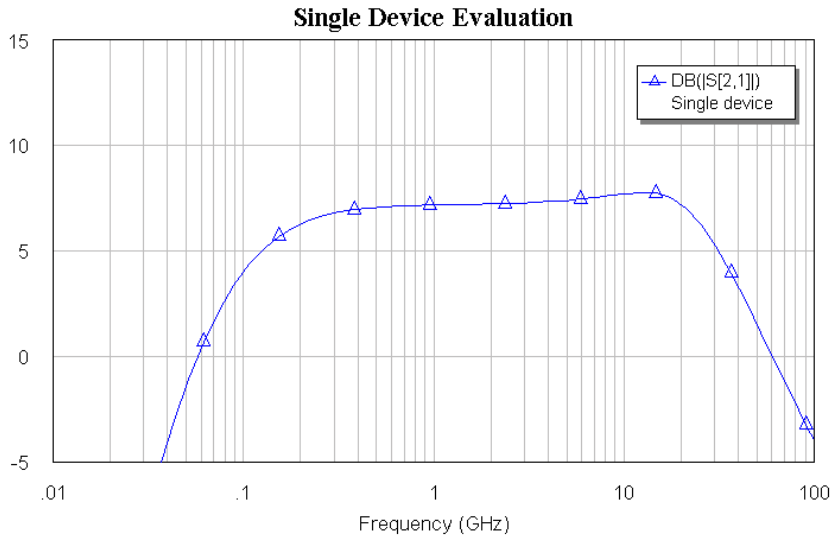


Figure 5: Model gain for amplifier Test 1

Figure 6 shows the measured input and output return loss in rectangular and Smith chart forms. As shown in Section 5, both input and output impedances are bias dependent, although not strongly so. Input and output return losses generally agree well with theory, although the input match is somewhat better than predicted. Amplifier Test 1's input matching resistors definitely improve the match at frequencies below 5-10 GHz.

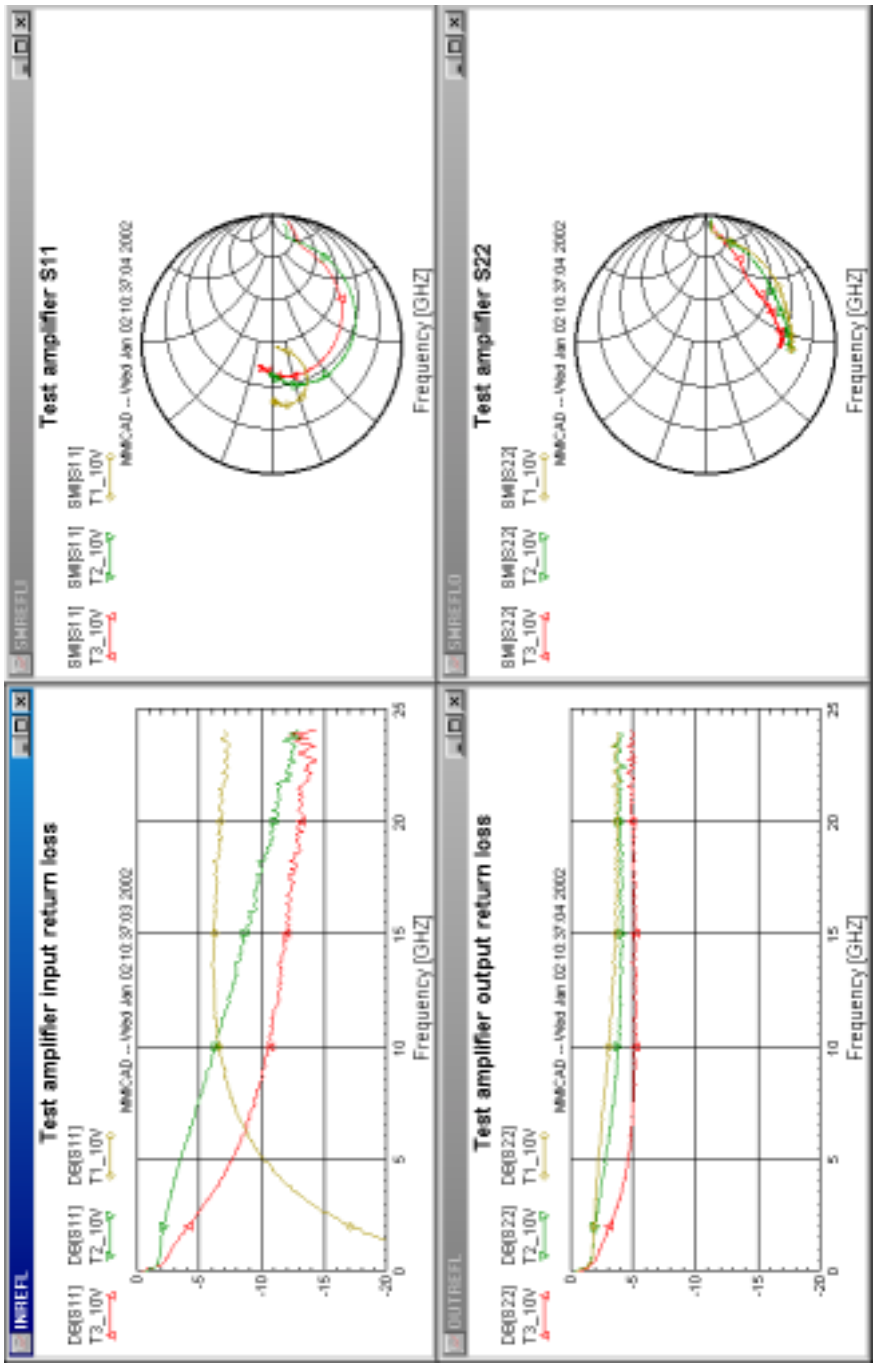


Figure 6: Input and output return loss for amplifiers Test 1, Test 2, and Test 3 at the nominal 10 V DC bias.

3 Tests for oscillation, amplifier Test 1

Although we haven't yet tried Sandy's suggestion of using a crystal detector, we have measured power levels in different bandwidths with a standard power meter and HP8481D power head (-70 dBm, 0-18 GHz) to check for power from oscillations below 20 or 30 GHz. This is a preliminary test to looking at the band with a spectrum analyzer and should be sensitive to oscillations at frequencies where bypassing the power supply would be of some help, at least.

The analysis checks for consistency with white noise across the band. For each filter, Table 2 gives the raw measured power; the gain-weighted fraction of power contained within each filter bandwidth; and the power within each band, corrected for the gain weighting. Numerical integration of the square of the voltage gain gives the gain weighting factors; these are normalized to unity for limits of integration from 0 to 22 GHz. The gain is still larger than unity at 22 GHz, and guessing at an extrapolation of the integrated power curve, it is possible to estimate that perhaps 85% of the power is below 22 GHz. The values in Table 2 includes neither this factor nor any deviations from ideal for the filter shapes, but these corrections are small and will not change the basic conclusions.

Filter	Measured Power [dBm]	Integrated power	Derived Power [dBm]
None	-55	1.01	-55
8 GHz LPF	-56	0.61	-54
2.2/1.3 GHz BPF	-65	0.11	-55

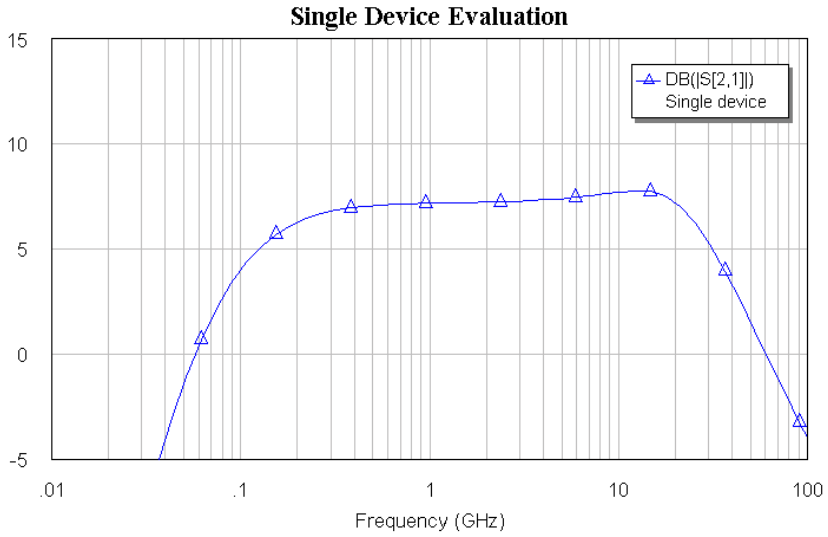
Table 2: Measured power,

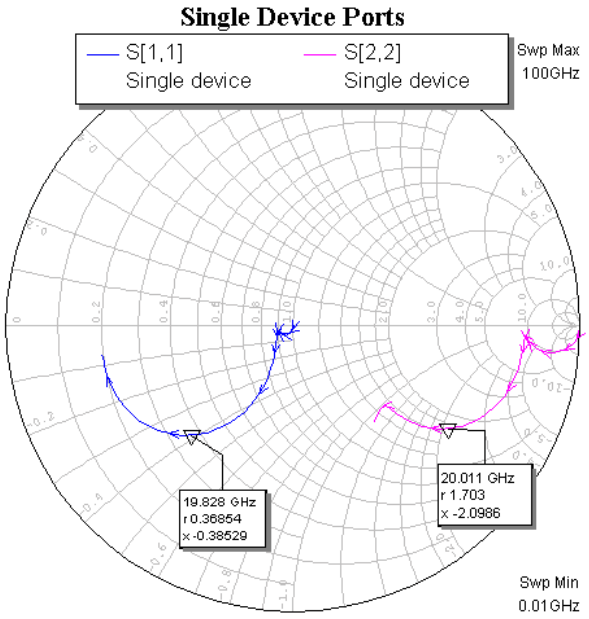
The last column in Table 2 is the power derived for the band assuming a flat noise spectrum: since these all agree well, either no oscillation is present over the range where the power detector is sensitive, the oscillation falls within a 1.3 GHz bandwidth centered on 2.2 GHz, or any oscillation does not make it out of the output port.

These measurements also allow an estimate of the amplifier noise figure. The average amplifier gain across the bandpass filter is 7.6 dB, so assuming 2 dB cable and probe loss the effective input power is –65 dBm – 7.6 dB + 2 dB = –71 dBm, or –101 dBW. From $P = kTB$, this corresponds to 4400 K, or an 11.8 dB noise figure.

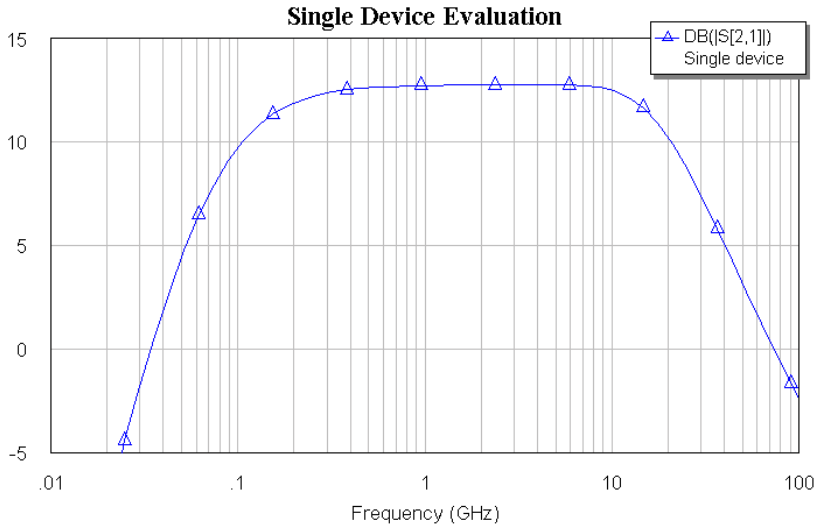
4 Modeling summaries

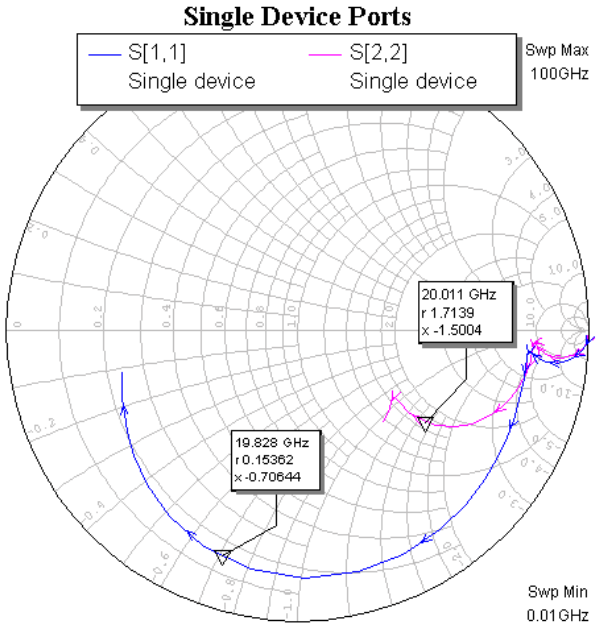
4.1 Test 1



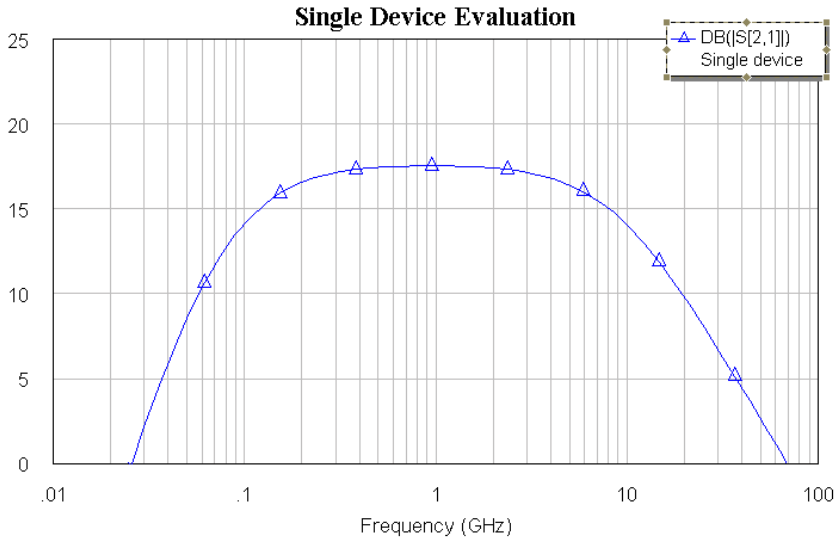


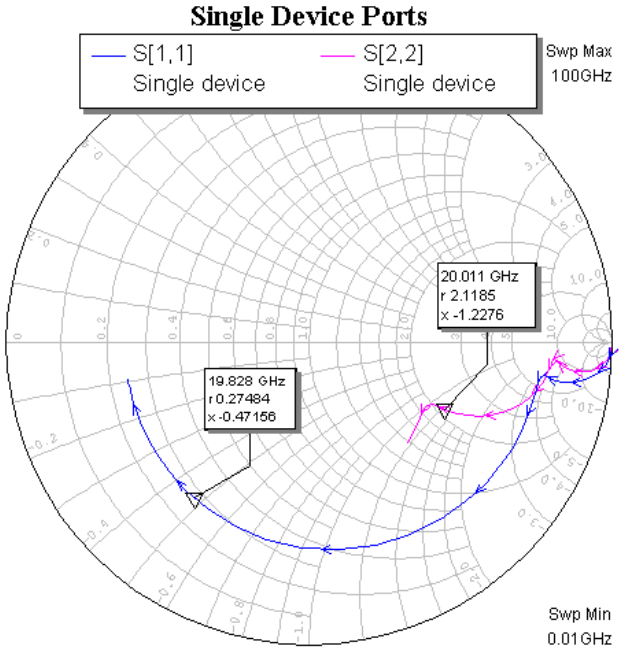
4.2 Test 2


Single Device Evaluation
DB(|S[2,1]|)
Single device
15
10
5
0
-5
.01
.1
1
10
100
Frequency (GHz)


Single Device Ports
S[1,1]
Single device
S[2,2]
Single device
Swp Max
100GHz
20.011 GHz
r 1.7139
x -1.5004
19.828 GHz
r 0.15362
x -0.70644
Swp Min
0.01GHz

4.3 Test 3


Single Device Evaluation
DB(|S[2,1]|)
Single device
25
20
15
10
5
0
.01
.1
1
10
100
Frequency (GHz)


Single Device Ports
S[1,1]
Single device
S[2,2]
Single device
Swp Max
100GHz
20.011 GHz
r 2.1185
x -1.2276
19.828 GHz
r 0.27484
x -0.47156
Swp Min
0.01GHz

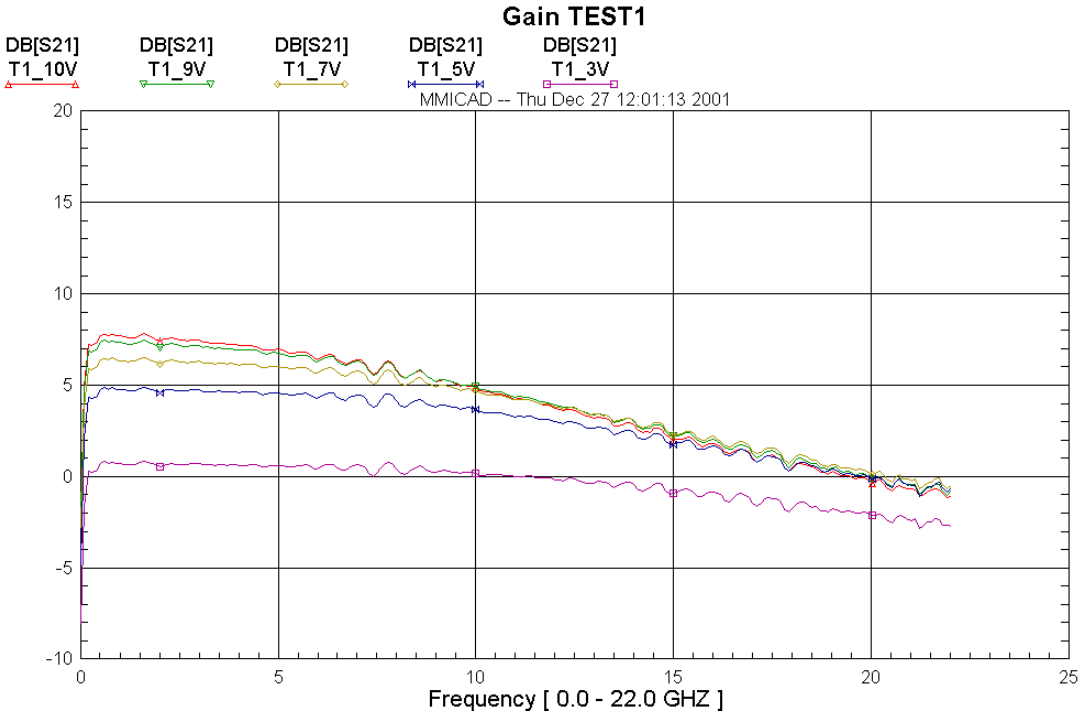
5 Bias current and S-parameters as functions of bias voltage

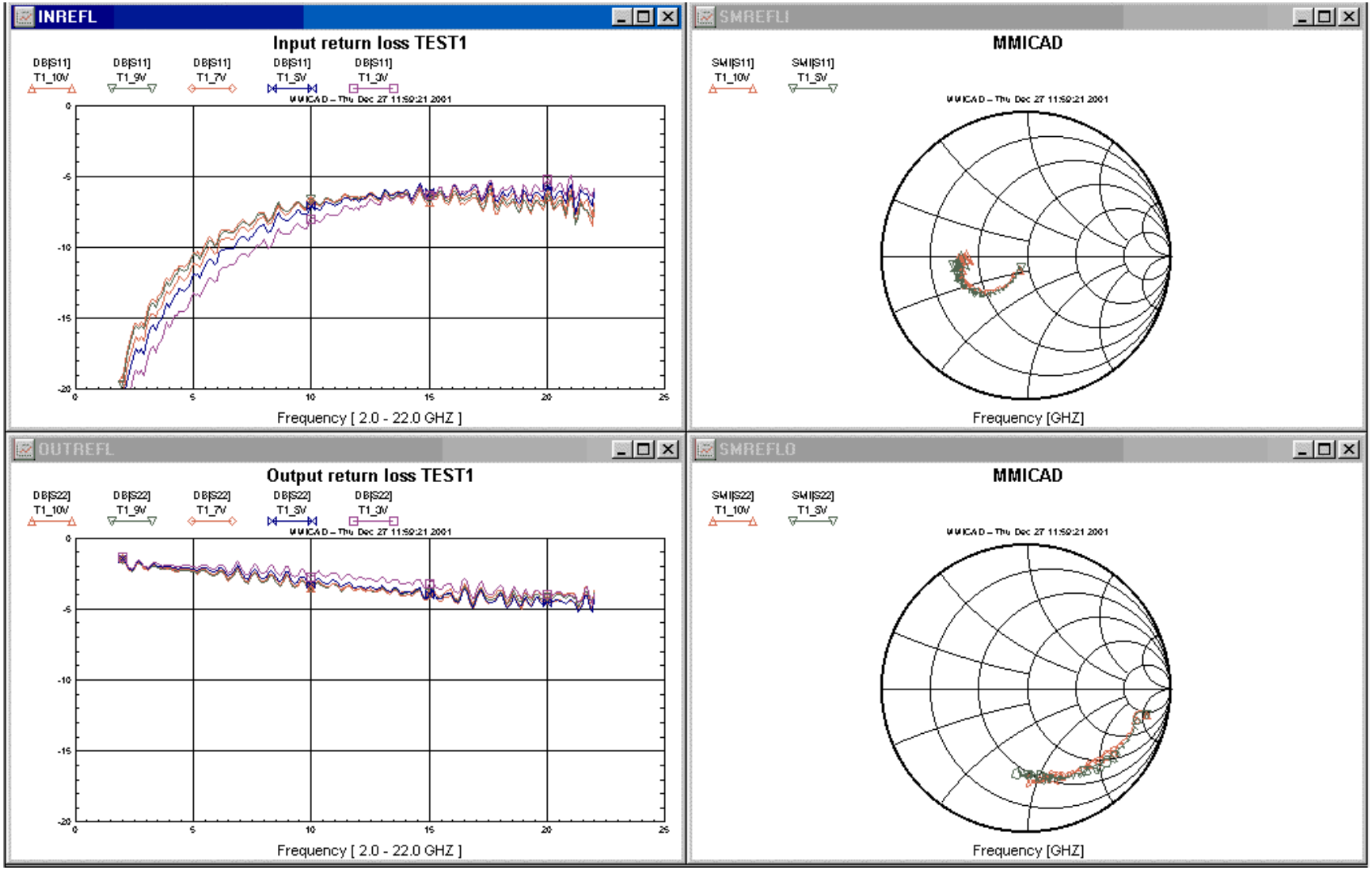
The following pages contain a summary of the first measurements of bias conditions and S_{21}, $S_{11,}$ and S_{22} for the test amplifiers. The key to the trace labels is simply illustrated by an example: T1_9V, for instance, corresponds to the Test 1 amplifier with a 9 V DC bias.

Microwave calibration for these measurements is through standard two line (standard and line 5) and short circuit TRL*/TRM* measurements on a GGB CS-5 calibration substrate. Calibration includes the probe constants supplied with the probes. Tests on short lines on the substrate showed reasonable values for S_{21} and S_{12}, with deviations of 0.2 dB p-p at high frequencies from a uniform slope of approximate magnitude 0.1 dB from 0.05 to 22 GHz. S_{11} and S_{22} also tested out well on and 25 and 100 Ω loads on the chip, with values clustered values around the nominal resistance within a couple of ohms at most frequencies. The measured impedances at the lowest frequencies, below 1 GHz or so, were obviously discrepant, presumably because the short line lengths for the calibration have inadequate phase differences for accurate calibration at the lowest frequencies. The SOLT calibration (Figure 3 and Figure 6) is superior.

5.1 Test 1

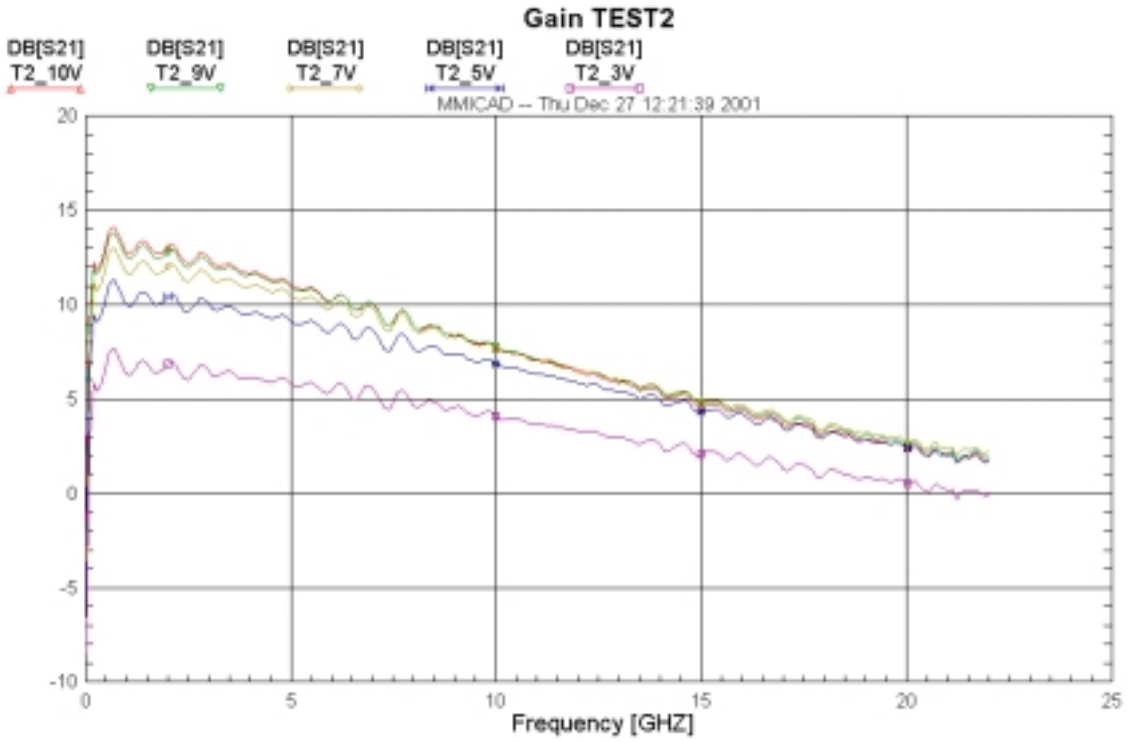
Voltage [V]	Current [mA]	File name
10.10	14.31	DATA07
8.97	11.84	DATA08
7.00	8.14	DATA09
5.05	5.01	DATA10
2.97	2.16	DATA11

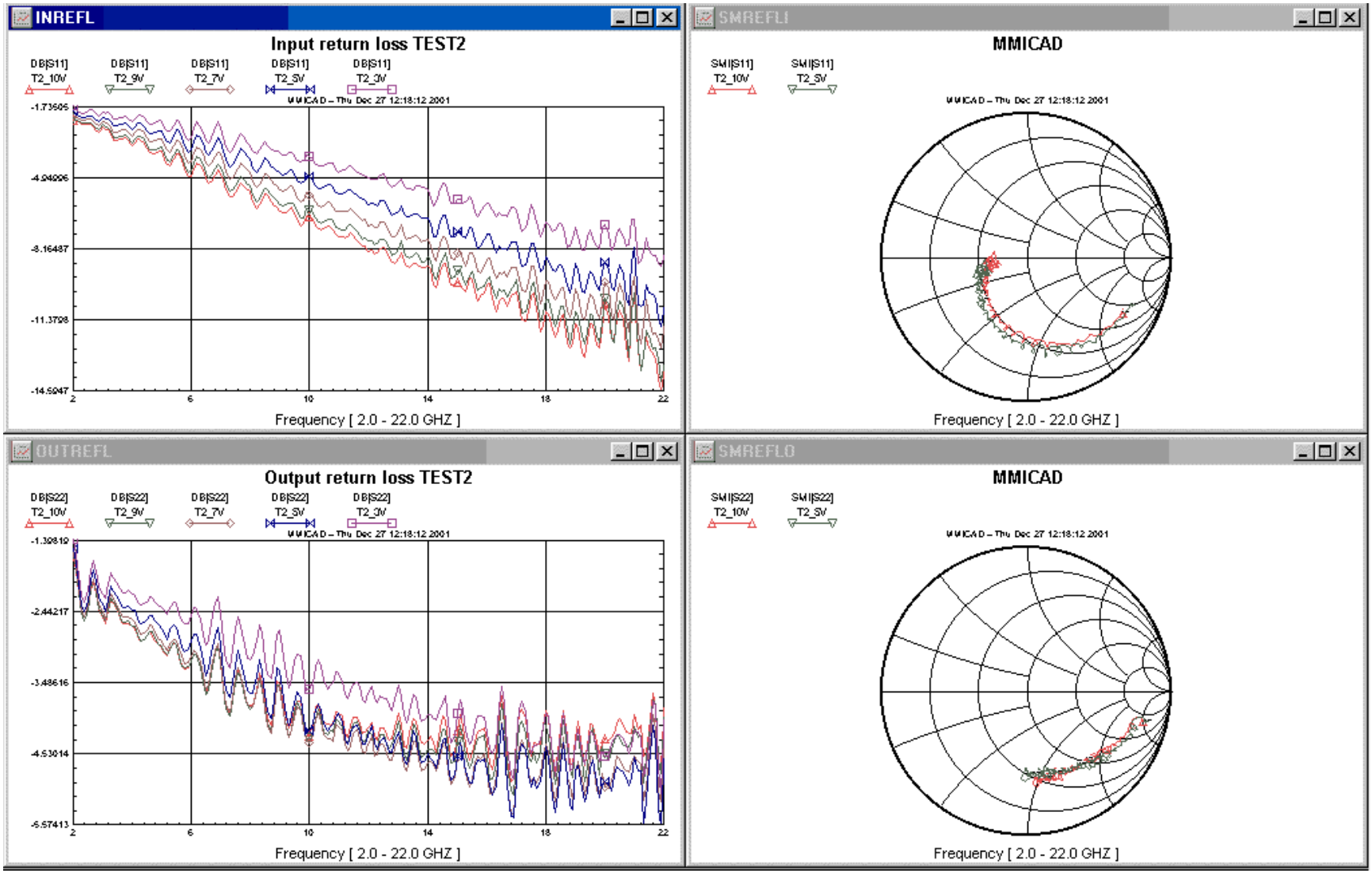



INREFL
Input return loss TEST1
DB[S11] T1_10V
DB[S11] T1_9V
DB[S11] T1_7V
DB[S11] T1_5V
DB[S11] T1_3V
MMICAD – Thu Dec 27 11:59:21 2001
0
-5
-10
-15
-20
0
5
10
15
20
25
Frequency [2.0 - 22.0 GHZ]
SMREFLI
MMICAD
SMI[S11] T1_10V
SMI[S11] T1_5V
MMICAD – Thu Dec 27 11:59:21 2001
Frequency [GHZ]
OUTREFL
Output return loss TEST1
DB[S22] T1_10V
DB[S22] T1_9V
DB[S22] T1_7V
DB[S22] T1_5V
DB[S22] T1_3V
MMICAD – Thu Dec 27 11:59:21 2001
0
-5
-10
-15
-20
0
5
10
15
20
25
Frequency [2.0 - 22.0 GHZ]
SMREFLO
MMICAD
SMI[S22] T1_10V
SMI[S22] T1_5V
MMICAD – Thu Dec 27 11:59:21 2001
Frequency [GHZ]

5.2 Test 2

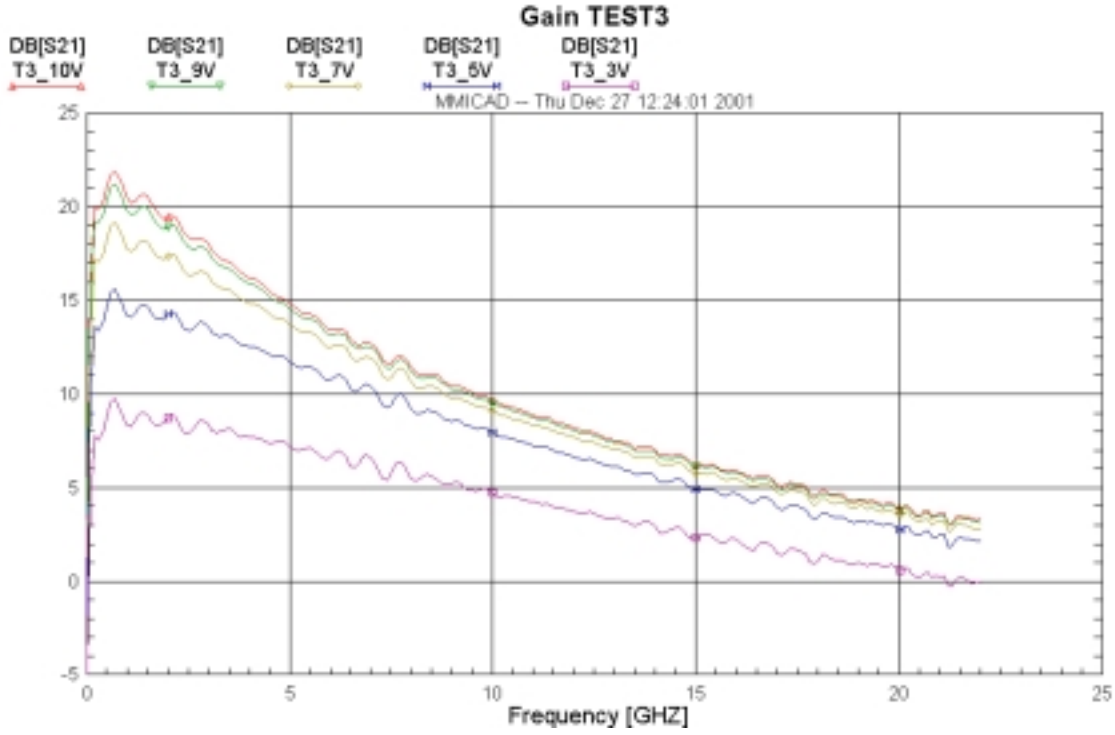
Voltage [V]	Current [mA]	File name
10.04	14.81	DATA15
8.96	12.57	DATA16
7.00	8.67	DATA17
4.96	5.20	DATA18
3.03	2.37	DATA19

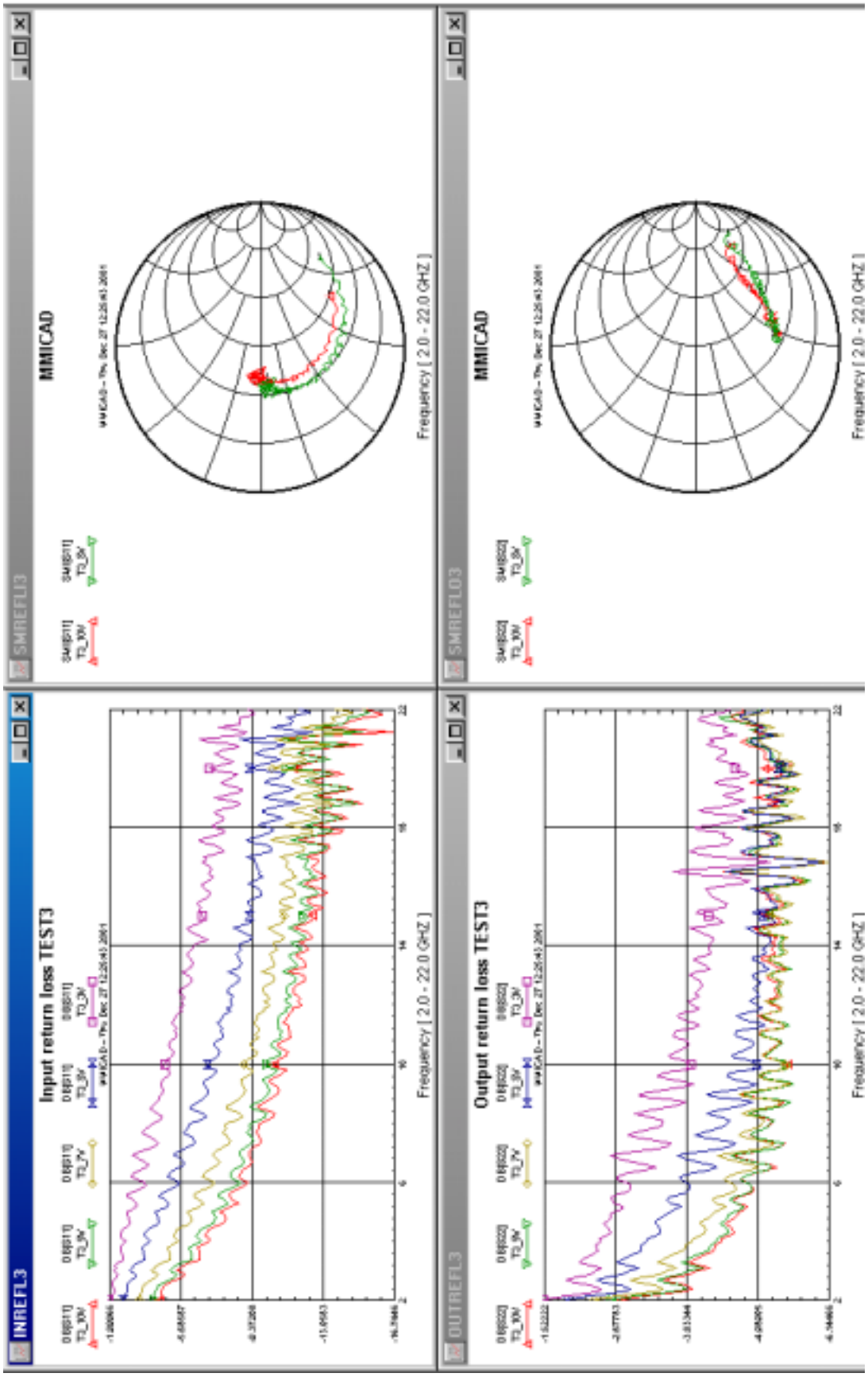



INREFL
Input return loss TEST2
DB[S11] T2_10V
DB[S11] T2_9V
DB[S11] T2_7V
DB[S11] T2_5V
DB[S11] T2_3V
MMICAD – Thu Dec 27 12:18:12 2001
-1.73505
-4.94906
-8.16487
-11.3708
-14.5847
2
6
10
14
18
22
Frequency [2.0 - 22.0 GHZ]
SMREFLI
MMICAD
SMI[S11] T2_10V
SMI[S11] T2_5V
MMICAD – Thu Dec 27 12:18:12 2001
Frequency [2.0 - 22.0 GHZ]
OUTREFL
Output return loss TEST2
DB[S22] T2_10V
DB[S22] T2_9V
DB[S22] T2_7V
DB[S22] T2_5V
DB[S22] T2_3V
MMICAD – Thu Dec 27 12:18:12 2001
-1.30819
-2.44217
-3.48616
-4.53014
-5.57413
2
6
10
14
18
22
Frequency [2.0 - 22.0 GHZ]
SMREFLO
MMICAD
SMI[S22] T2_10V
SMI[S22] T2_5V
MMICAD – Thu Dec 27 12:18:12 2001
Frequency [2.0 - 22.0 GHZ]

5.3 Test 3

Voltage [V]	Current [mA]	File name
10.07	16.71	DATA00
8.99	13.94	DATA01
7.00	9.11	DATA02
4.99	5.06	DATA03
3.01	2.21	DATA04




SMREFL3
MMICAD
Frequency [2.0 - 22.0 GHZ]
SMREFL03
MMICAD
Frequency [2.0 - 22.0 GHZ]
INREFL3
Input return loss TEST3
Frequency [2.0 - 22.0 GHZ]
OUTREFL3
Output return loss TEST3
Frequency [2.0 - 22.0 GHZ]