CARMA Memorandum Series #13

[DRAFT] DAQcore: a General Purpose Data Acquisition CANbus Node

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ABSTRACT

This memo contains a detailed description of a general purpose data acquisition CANbus node developed by the author at the RAL. The planned uses of this node include the monitoring and control of the correlation water vapor radiometer, and the CARMA IF amplifier and related fiber optic components. The module is general enough, however, to be useful in many other applications.

Change Record

Revision	Date	Author	Sections/Pages Affected
	Remarks		
0.9	2003-Sep-01	A. Bolatto	1-16
	Initial draft release. Comments are welcome.		

1. Motivation

With the integration of CARMA a lot of emphasis has been put into distributing control functions among microcontrollers capable of communicating with a central computer using the CANbus (Controller Area Network) standard. Taking advantage of the experience at OVRO, we based our design on the Phytec phyCORE-PXAC3 single board computer (SBC) implemented using a Philips XAC-3 microprocessor to be at the base of every node. The practice up to now has been to embed the SBC into almost every new piece of hardware, which requires reengineering the interface between the SBC and its environment for each application. An alternative path is to have a standard, well debugged, well understood node that provides the fundamental data acquisition and control capabilities. Such a standard node may only need some additional signal conditioning hardware, and could be used in almost every situation.

The DAQcore module discussed here was designed to control the water vapor correlation radiometers under development at the RAL in Berkeley, but it is general enough to be useful in many other applications: for example, it will provide the monitor and control functions in the CARMA IF module also under development at the RAL. The DAQcore provides 8 differential 16-bit analog inputs (expandable to 512) connected to a fast (500 Ksamples/s) A/D converter, 8 channels with 14-bit analog outputs, 16 digital inputs, and 16 digital outputs. Thus, its capabilities probably exceed those required by most applications. The most expensive ICs are the A/D and D/A, each costing \$50—\$60, and they can be left unpopulated if the application does not require them. The footprint of the card is $6'' \times 3''\frac{3}{8}$ with a height of $\frac{3}{4}''$.

2. Detailed Description of Capabilities

2.1. Analog Input

The DAQcore module provides 8 fully differential analog inputs. These inputs are multiplexed by two on–board ADG528F analog switches, one for the $V+$ and one for the $V-$ channel, manufactured by Analog Devices. The $V+$ and $V-$ channels are then input into an AD622 instrumentation amplifier with gain unity, which provides high common mode rejection as well as a common mode output, referenced to +1.20 V provided by a LT1004-1.2 reference diode. The output of this amplifier is available at test point TP4. Following the instrumentation amplifier is a 4th order low pass Bessel filter implemented using an OP270EZ dual precision operational amplifier (output available at TP6). The cutoff frequency of the filter is high, 300 to 600 KHz, and its purpose is to provide high frequency noise reduction.

Values of the components for different cutoff frequencies are found in Table I. Because the filter is after the multiplexer, its cutoff frequency restricts the speed with which channels can be switched. A Bessel topology was chosen to preserve the waveform after the switch, thus minimizing the induced cross–talk between channels. The Sallen–Key implementation used for the filter guarantees that its DC gain is unity, which avoids having to individually calibrate the gain of each DAQcore module. The gain accuracy of the input amplifier is thus the limiting element, with a typical value of $\sim 0.05\%$ (worst case 0.15%). Accuracy beyond this factor requires calibration of the individual boards.

The analog signal is digitized by an AD7676 IC. This is a new generation successive–approximation charge–redistribution A/D converter, capable of digitizing 500 Ksamples per second with 16 bit resolution and excellent linearity. Unfortunately, its analog input is a bit more difficult to drive than I would like: it accepts a ±2.5 V differential input range, but each of the differential inputs can only swing between 0 and +3 V. Thus driving it over its full potential range requires a differential output precision amplifier, which are difficult to come by (differential output amplifiers are commonly used to drive twisted pairs in audio or high speed data communications, like DSL modems, but those are not precision amplifiers). Thus, for practical reasons we have to restrict the input range: the available differential input range of the analog inputs is ±1.2 V (it appears to be linear over ±1.5 V). The resolution of the converter is 16 bits over 5 volts, or 76.3 μV per count.

2.1.1. Properties of the input stage

Applying differential or common mode voltages as high as ±15 V to the input of the analog amplifiers will not damage the circuit, since the inputs of the AD7676 are protected by clamp diodes and the OP270 used to drive these inputs is not capable of sourcing enough current to damage them. Similarly, the input analog switches are fault and overvoltage protected to -40 to $+55$ V and clamp their output voltages to their power supply if an overvoltage condition occurs. Thus, it is unlikely that any voltage in that range applied to any of the analog inputs would damage the board components, and the board should recover without requiring a reset or a power cycle.

The ADG528F switches were chosen not only because of their overvoltage protection, but also because they are latch–up proof (i.e., they will switch even if their inputs have an overvoltage applied), they guarantee break before make contact, and they include their own decoders. Their settling time is specified to be 2.5 μs to 0.01%, which appears to be an excellent match to the AD7676 maximum conversion rate. They provide an isolation between channels of > 50 Db, which guarantees that the channel cross–talk due to the switch will stay below 1

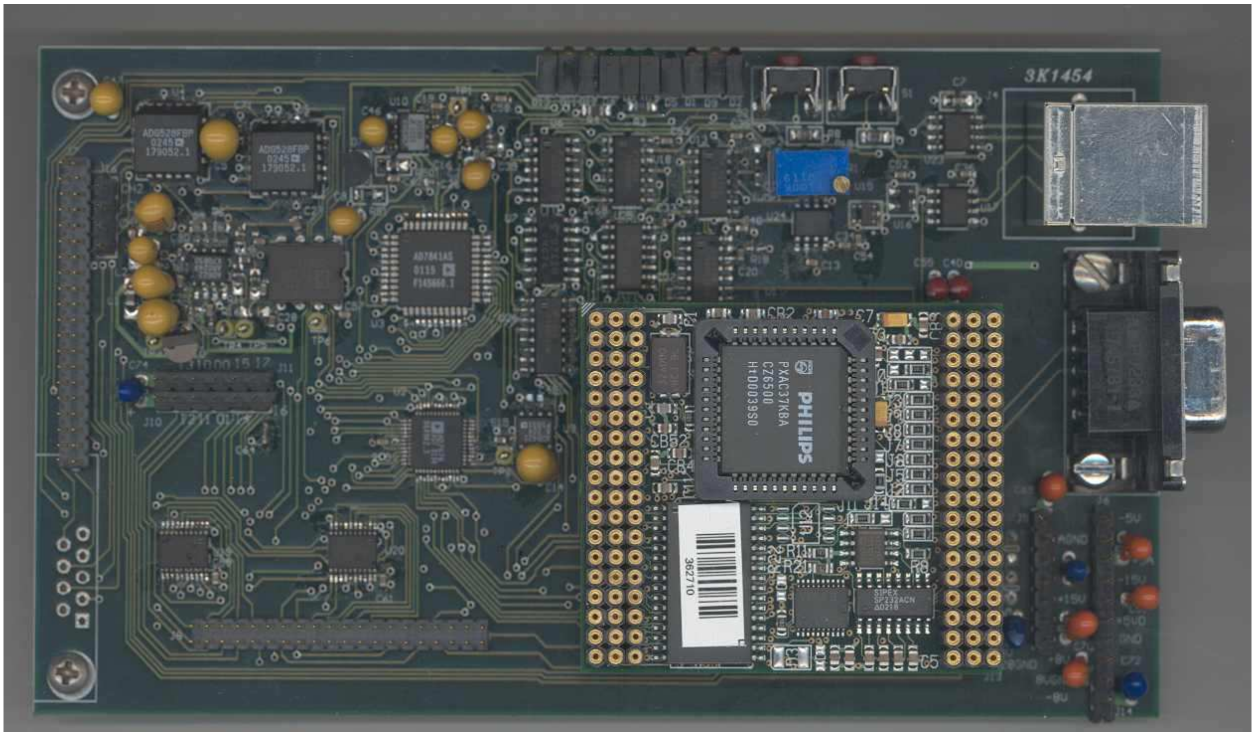

Fig. 1.— DAQcore module

Table I: Input Filter Components

Cutoff fq.	R11	R12	C18	C27	R14	R16	C29	C28
600 KHz	2.26 KΩ	21.5 KΩ	47.0 pF	15.0 pF	2.21 KΩ	18.2 KΩ	68.0 pF	10.0 pF
300 KHz	2.15 KΩ	19.6 KΩ	100.0 pF	33.0 pF	2.00 KΩ	16.5 KΩ	150.0 pF	22.0 pF
150 KHz	1.96 KΩ	18.7 KΩ	220.0 pF	68.0 pF	1.82 KΩ	15.4 KΩ	330.0 pF	47.0 pF
50 KHz	1.91 KΩ	17.4 KΩ	680.0 pF	220.0 pF	2.61 KΩ	22.1 KΩ	680.0 pF	100.0 pF
10 KHz	1.96 KΩ	19.1 KΩ	3.3 nF	1.0 nF	1.91 KΩ	16.2 KΩ	4.7 nF	680.0 pF

ADC count.

The AD622 and the OP270EZ were chosen because of their excellent input offset voltage and current specifications, and because they are inexpensive. The settling speed of the AD622, alas, is probably the limiting parameter when switching between channels or digitizing very fast signals. Its settling time to 0.01% may be as slow as $\sim 10\ \mu$s (the specifications in the data-sheet, however, do not quite address this point; 10 μs is the settling time for a large voltage swing and it is dominated by the slew rate). This suggests that to obtain a cross–talk of order 1 ADC count a delay of $\sim 10\mu$s may have to be introduced between switching input channels and starting the analog–to–digital conversion.

The input impedance of the AD622 is 10 GΩ. To guarantee the correct working of the AD622 independent of the voltage source connected at its input, however, we provide a path for the bias current through 560 KΩ resistors to ground (bias resistors). This reduces the input differential impedance to ~ 1 MΩ. If this is a problem the input resistors can be eliminated by not populating them in the board. The price to pay for this approach is that the output of the AD622 will most likely swing to one of its rails when no voltage is applied to its inputs, a condition which may affect its dynamic performance given its limited slew rate. The bias resistors are dimensioned to keep the offset voltage due to the input offset current to ~ 0.5 mV, comparable to the output offset voltage of the AD622, which is 0.6 mV. Thus, the total DC offset voltage of the circuit may be up to ~ 1 mV. The zero point offset measured in our prototype was 0.2 mV (Figure 2). This offset could be calibrated and stored in the EEPROM memory of each board if better DC zero–point accuracy is desirable. In fact, it could be calibrated out in real time by leaving one of the input channels shorted, and measuring it frequently.

2.1.2. Microprocessor interface and channel expansion

The conversion control line of the AD7676 is connected to pin 3.4 (`T0` output) of the XAC3 through a one-shot circuit that generates a valid conversion start pulse every time there is a falling edge in the `T0` line. During the conversion the `BUSY` line line of the AD7676 goes up. When it falls it brings down pin 3.2 ($\overline{\texttt{INT0}}$ input) of the XAC3, which generates an event interrupt in the microprocessor if the interrupts are enabled. The $\overline{\texttt{CS1}}$ line of the Phycore module is used to decode the memory mapped output of the AD7676. Reading this memory address (0xFFD00 in hexadecimal) will automatically clear the interrupt and bring the $\overline{\texttt{INT0}}$ input to its neutral (high) state.

The lowest three bits (data bus lines 0—2) written to the memory address of the ADC will

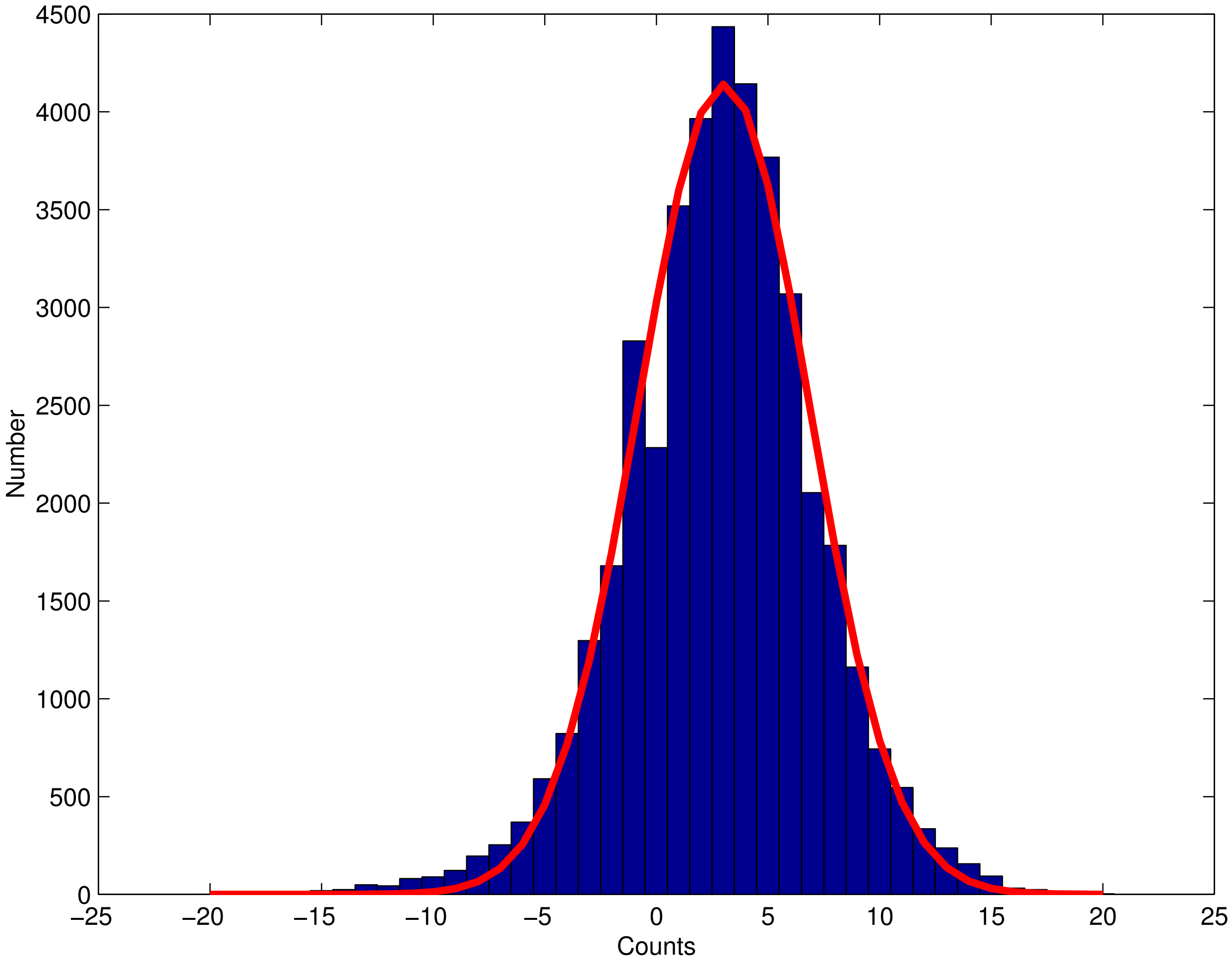

Fig. 2.— Noise measured in a long series of measurements of channel 0 in the prototype, with its inputs shorted. The output offset measured was 216 μV, with a maximum rate of change of 10 μV/hr (probably due to temperature). The standard deviation of the samples was 320 μV. No shielding was present, and the inputs were shorted using a long cable.

select its input channel. Lines 3—8 of the XAC3 data bus are buffered and provided at the 20 pin header connector J7, together with a buffered decoder line BCS used to decode the ADG528F. These lines could be used to address a bank of up to 8 × 8 × 2 external ADG528F switches, for example, providing a grand total of 512 differential input channels to the AD7676. A second chip select decoder signal BGS is activated by writing to address 0xFFF00. The purpose of this signal is again to be used with external latches (such as the ones in the ADG528F) to write values to external components. The difference between BCS (buffered channel select) and BGS (buffered gain select) is that BCS will be activated every time an input channel is switched, while BGS is separate from switching channels. This is important for some applications (like changing the gain of an external circuit), where we want to avoid glitches to occur every time we switch a channel.

2.2. Analog Output

The DAQcore module provides 8 common mode unipolar analog outputs. These are produced by an AD7841 14–bit resolution digital–to–analog converter. Six of these outputs (channels 0—5) use +5.00 V references and can output voltages between 0 and +10 V, while the last two outputs use -1.20 V references, thus they can produce voltages between -2.4 and 0 V. The AD7841 is an easy to use IC, with internal channel decoding. Its outputs can swing up to 2.5 V of its power supplies, and source up to 15 mA with a slew rate of 0.7 V/μs. The linearity and zero point errors of the ADC7841 are ±8 counts worst case (5 and 1.2 mV respectively).

Following a power up the outputs of the AD7841 are forced to zero by an asserted $\overline{\texttt{CLR}}$ signal in its pin 29. This should be a “safe” voltage, and guarantees that no damage will be done to external equipment connected to the DAQcore during power cycles. Releasing the $\overline{\texttt{CLR}}$ signal requires a read from the memory mapped address of the D/A converter, which should be done only after writing valid output values to its channels.

The $\overline{\texttt{CS2}}$ line provided by the Phycore module is used to decode the memory mapped registers of the AD7841. The 14 bit registers corresponding to the values of the 8 output channels are mapped in consecutive addresses from 0xFFE00 to 0xFFE10. Writing to these addresses will set the corresponding output of the DAC. Reading from any of these addresses will release the $\overline{\texttt{CLR}}$ signal asserted by a power cycle or a reset.

2.3. Digital IO

In connectors J7 and J8 the DAQcore module provides 16 digital inputs, 16 digital outputs, and 4 I/O pins directly connected to the XAC3 (P1.4, P1.5, P1.7, and P3.3). The pins corresponding to the outputs of the three XAC3 internal timers (P3.4, P3.5, and P1.6) are also available externally, and two of these are independently buffered and available as BT1 and BT2. Pin 1.7 has been provided with a 5 KΩ pull up resistor, to be used as a bidirectional pin for 1–wire devices (such as the DS2401 silicon serial number ID ICs).

The 16 digital inputs are implemented using 74VHC245 transceivers, decoded by the $\overline{\texttt{CS3}}$ Phycore line and mapped to the memory address 0xFFF04. A read to this address will return the status of the 16 input lines in the two 74VHC245 transceivers. A write to this address will output a value through the 74VHC373 latches used to implement the 16 digital outputs. The output of the latches will be in high–impedance mode following a power cycle or a reset, until the user enables the outputs of the DAQcore module by reading from address 0xFFE00 (as described in the previous section). The upper nibble of the word at this location (bits 12 to 15) has a special function: bits 12—15 are connected to yellow LEDs, and bit 15 is used to enable or disable the external timer mechanism.

2.3.1. External interrupt timer

In the scheme adopted by CARMA the individual CANbus nodes are responsible for reporting to the central computer every 500 ms, within a window of [-50,+100] ms on the tick, without any external querying. Nodes that miss the reporting window will be assumed to be non–functioning. The time synchronization mechanism is based on a once a second pulse (1 pps) distributed using two pins of the CANbus connector (the “missing pulse”). The problem then is to generate a twice a second reporting interrupt based on a once a second time signal. One possible solution is to devote one of the XAC3 internal timers to time keeping chores, a resource that would then be unavailable for other tasks. The alternative solution employed in the DAQcore is to have an external timer synchronized to the missing pulse signal produce the 0.5 s reporting interrupts. The external timer is implemented using a 555–type IC with an RC time constant of 0.5 s. Its reset input is connected to the 1 pps distribution, thus restarting the charging of the timing capacitor and synchronizing the integer second interrupts to the 1 pps signal. Because it is impossible to guarantee 10% timing with the typical 20% dispersion in the capacitor values, a variable potentiometer is provided to adjust the timing of the 555. The output of the external timer is connected to the INT1 line of the XAC3 through a one–shot.

The interrupts provided by this external timer circuit can be turned on and off by setting and reseting bit 15 of the digital output port. The external interrupts in the XAC3 are level sensitive, thus they persist until the input that caused them (i.e., the stimulus) goes high. This means that if the stimulus is still present, the interrupt handler routine will be reentered upon exit, essentially precluding normal tasks from running. The way of removing the stimulus provided in this case is to toggle digital output bit 15, which will reset the 74VHC123A one–shot generating the interrupt. The one–shot, of course, will clear itself after a while, but if the interrupt handler routine is extremely fast this may not happen soon enough. When the external timer interrupts are enabled (`DO15`=1) the yellow LED D9 will blink at their rate. While they are disabled (`DO15`=0) LED D9 will be off, and pin 3.3 of the XAC3 will be available for other uses.

3. Supply Voltages

The DAQcore module requires four power supplies and two grounds: +5 V digital, +5 V analog, +15 V, −15 V, digital ground, and analog ground. The digital +5 V is the most widely distributed supply. The analog +5 V is only used by the AD7676 A/D converter, and it could be shorted to the digital +5 V in the power supply connector if the application can tolerate the possibility of extra noise in the digitizing of analog signals. The nominal ±15 V power supplies are used by the analog components, including the D/A converter, the ADG528F switches, and the input amplifier/filter stage, and there is some range in the actual tolerable voltages. It is possible to run the DAQcore with ±14 V generated using 24–to–15 V DC–to–DC converters and low–dropout linear regulators. This will be probably the default CARMA mode. Providing voltages of less than +13 V will start compromising the output range of the D/A converter, which needs +2.5 V of headroom for its output amplifiers.

The AD7841 IC has some restrictions in its power supply sequencing. In particular, it cannot tolerate a large difference between its VDD (+15 V) and VCC (+5 V) inputs (VCC cannot be applied without VDD). The DAQcore is equipped with power clamping diodes (D6A and D6B) to prevent damage to this IC from power supply transients during power up, but I cannot guarantee that they will be able to indefinitely withstand +5 V being applied with no +15 V. When using this module please supply all the relevant voltages.

3.1. Interfaces

The DAQcore provides several connectors to interface with the rest of the world. The power supply header connectors, J5 and J6, are internally connected and can be used to daisy chain the power supplies of several modules. The standard communication connectors for RS232 and CANbus are provided in J3 and J4, the latter without a T–split in the module since there was no space for it. The main output connectors are two 40–pin 0.1" spacing headers for ribbon cable, one of them carrying only digital signals (J8), and the other carrying a mixture of digital and analog (J7). In addition to these there are a few other header and DB type connectors that are intended for special use in the IF module control, but that are also available for general use.

The front "panel" of the DAQcore module has two pushbuttons, provided for manual RESET and BOOT functions, a well as an array of LEDs. The general philosophy concerning the coloring of the LEDs is that green LEDs should be always on during normal functioning, red LEDs should be always off, and yellow LEDs have meanings that are module and programming dependent. The four green LEDs in the DAQcore are connected to the power supplies, and they show that normal voltages are applied. The red LEDs are connected to the RESET and BOOT lines (including the external RESET at the CANbus connector), and turn on only when these lines are active. Of the 4 yellow LEDs, 3 are uncommitted (connected to digital outputs 12 to 14) and the fourth should blink at the rate of the external interrupt timer, if the timer is enabled by setting digital output 15 to one.

4. Software

A library of basic functions has been provided for the DAQcore, contained in the `daqio` module created by me. These include functions to initialize the module (e.g., the ADG528F switches nominally need a longer $\overline{\texttt{WR}}$ pulse than that provided by default by the XAC3. This

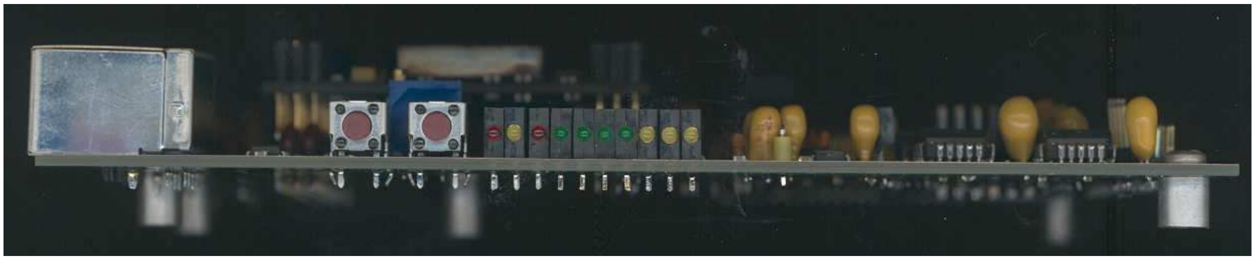

Fig. 3.— DAQcore front panel: RESET and BOOT pushbuttons and LEDs.

Table II: DAQcore Memory Map

0xFFD00—0xFFD01	READ:	A/D conversion result (16 bits, two's complement)
		& clear $\overline{\texttt{INT0}}$
	WRITE:	Set channel 0. . . 7 internal
		Set channel 0. . . 512 expansion
0xFFD02—0xFFDFF		Mirrored 0xFFD00—0xFFD01
0xFFE00—0xFFE01	READ:	Release CLR latch to AD7841 and DO
	WRITE:	Set D/A channel 0 output (14 bits, unsigned)
0xFFE02—0xFFE03	READ:	Mirrored 0xFFE00—0xFFE01
	WRITE:	Set D/A channel 1 output (14 bits, unsigned)
0xFFE04—0xFFE05	READ:	Mirrored 0xFFE00—0xFFE01
	WRITE:	Set D/A channel 2 output (14 bits, unsigned)
0xFFE06—0xFFE07	READ:	Mirrored 0xFFE00—0xFFE01
	WRITE:	Set D/A channel 3 output (14 bits, unsigned)
0xFFE08—0xFFE09	READ:	Mirrored 0xFFE00—0xFFE01
	WRITE:	Set D/A channel 4 output (14 bits, unsigned)
0xFFE0A—0xFFE0B	READ:	Mirrored 0xFFE00—0xFFE01
	WRITE:	Set D/A channel 5 output (14 bits, unsigned)
0xFFE0C—0xFFE0D	READ:	Mirrored 0xFFE00—0xFFE01
	WRITE:	Set D/A channel 6 output (14 bits, unsigned)
0xFFE0E—0xFFE0F	READ:	Mirrored 0xFFE00—0xFFE01
	WRITE:	Set D/A channel 7 output (14 bits, unsigned)
0xFFE10—0xFFEFF		Mirrored 0xFFE00—0xFFE0F
0xFFF00—0xFFF01	WRITE:	Set external gain (bits 3. . . 8)
0xFFF02—0xFFF03		Unassigned
0xFFF04—0xFFF05	READ:	Get digital input word (16 bits)
	WRITE:	Set digital output word (16 bits)
		Bits 0. . . 11 uncommitted
		Bits 12. . . 14 LEDs
		Bit 15 turn external timer on/off & clear $\overline{\texttt{INT1}}$
0xFFF06—0xFFFFF		Mirrored 0xFFF00—0xFFF05

is easily solved by programming one of the Phycore registers), to program the XAC3 internal timers, and to use the A/D, D/A, and digital IO, including the LEDs. The documentation has been embedded in the code and there is a hypertext version accessible online that was created using Doxygen. This is a short list of various useful functions:

Initialization

init_daq Properly initialize the AD7841 registers, activate its output, and program the Phycore external bus so it can talk to the ADG528F switches.

Access to the A/D

trigger_adc Switches the ADG528F to the corresponding channel and triggers a conversion at the AD7676.

read_adcvol Waits for the current conversion to finish and returns the readout of the AD7676 converted to volts.

sample_channels Triggers successive conversions in a list of channels with the requested rate, until obtaining the specified number of samples. The individual voltages measured are stored in a user–supplied buffer. It has two modes of operation: normal mode, in which the channels are switched in at the rate specified, or burst mode, where at every tick of the timer it will go through the entire list of channels at the fastest possible channel switching frequency (i.e., produce quasi–simultaneous channel measurements). This routine uses the XAC3 timer 0 and will reprogram it.

Access to the D/A

write_dacvol Output a voltage in a particular channel of the D/A.

Digital IO

set_extgain Activate the `BGS` signal, provided to select a gain with an external latch.

read_dio Read a 16–bit word from the DIO address.

write_dio Write a 16–bit word to the DIO address.

write_led Write a 0–7 value to turn the LEDs on/off. It leaves the other outputs unaffected.

write_udo Write a value to the 12 “uncommitted” lowest bits of the DIO, leaving bits 12—15 unchanged.

set_bitdio Set a particular bit in the digital output.

clr_bitdio Clear a particular bit in the digital output.

toggle_bitdio Toggle a particular bit in the digital output.

Timer control

start_timer Start a XAC3 timer to generate overflows with a given frequency. It can also output a square wave in the corresponding pin.

stop_timer Stop a XAC3 timer.

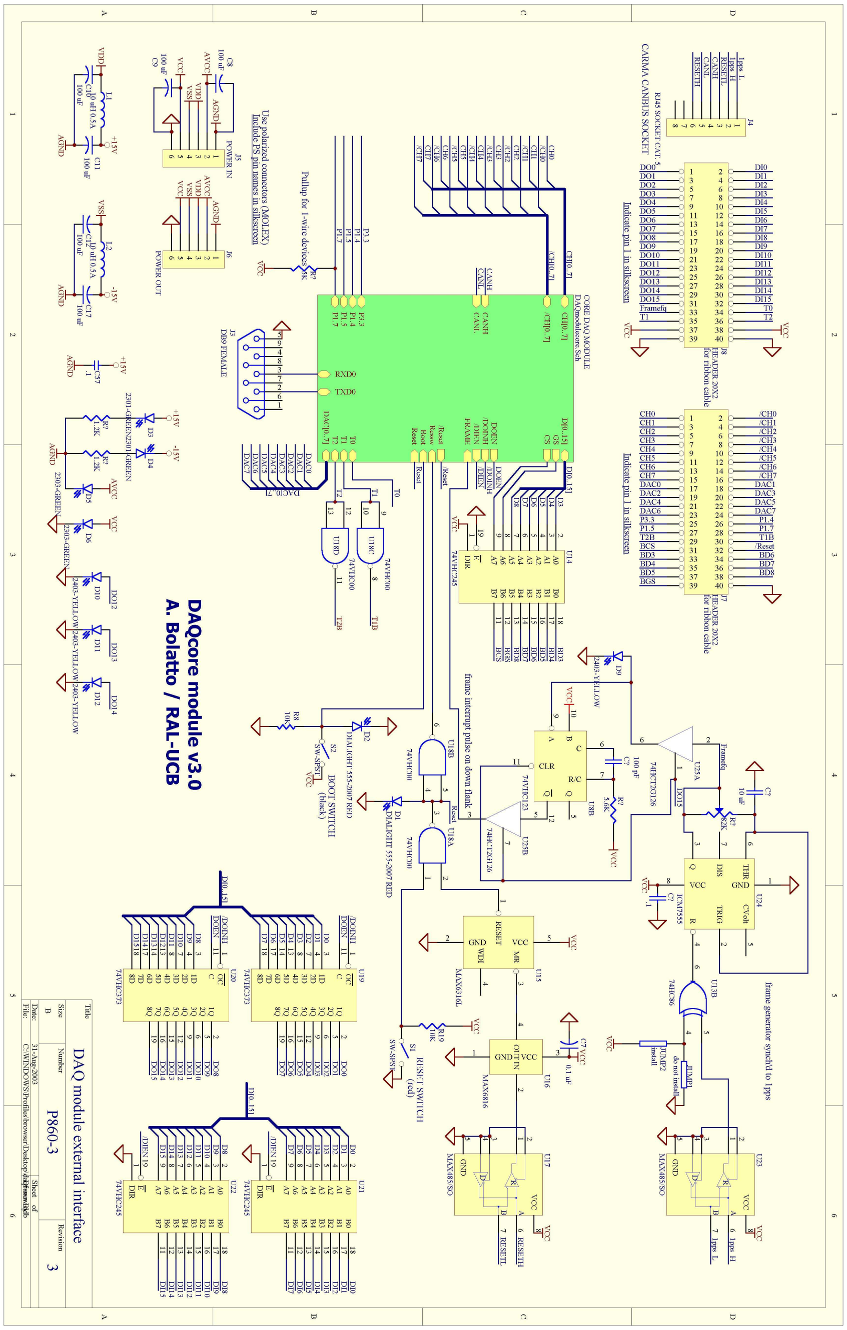

Fig. 4.— DAQcore module external interfaces, including digital IO.

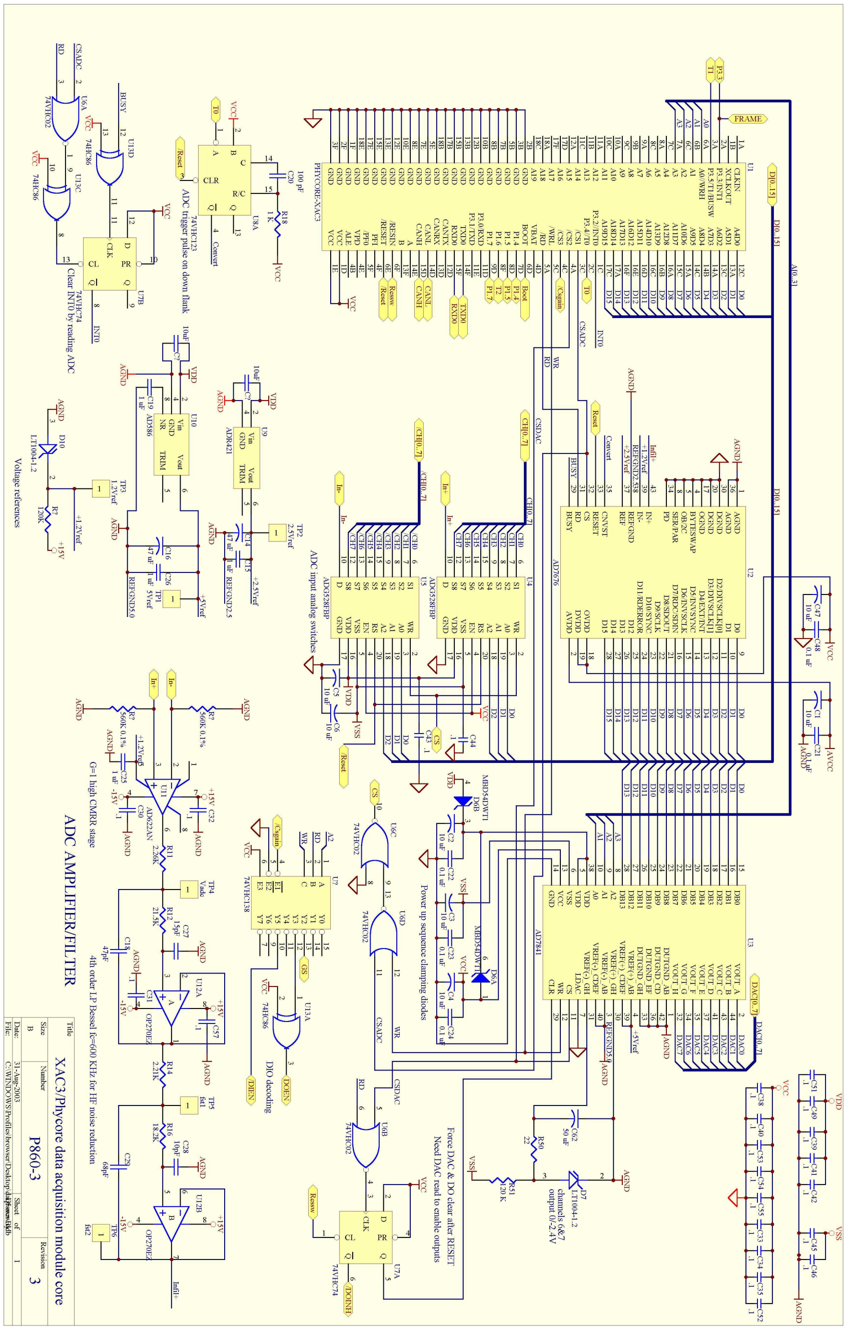
ADC AMPLIFIER/FILTER
ADC trigger pulse on down flank
Clear INT0 by reading ADC
Voltage references
ADC input analog switches
G=1 high CMRR stage
4th order LP Bessel fc=600 KHz for HF noise reduction
Power up sequence clamping diodes
DIO decoding
Force DAC & DO clear after RESET
Need DAC read to enable outputs
PHYCORE-XAC3
AD7676
AD7841
ADG528BRP
AD8221AN
OP270EZ
ADR421
AD586
LT1004-1.2
74VHC123
74VHC74
74VHC02
74VHC86
74VHC138
Title
XAC3/Phycore data acquisition module core
Size
B
Number
P860-3
Revision
3
Date:
31-Aug-2003
Sheet 1 of 1
File:
C:\WINDOWS\Profiles\browse\Desktop\daqcore.ddb

Fig. 5.— DAQcore module A/D, D/A, and decoding.