M4 MCU Testing

Research done for Texas Instraments

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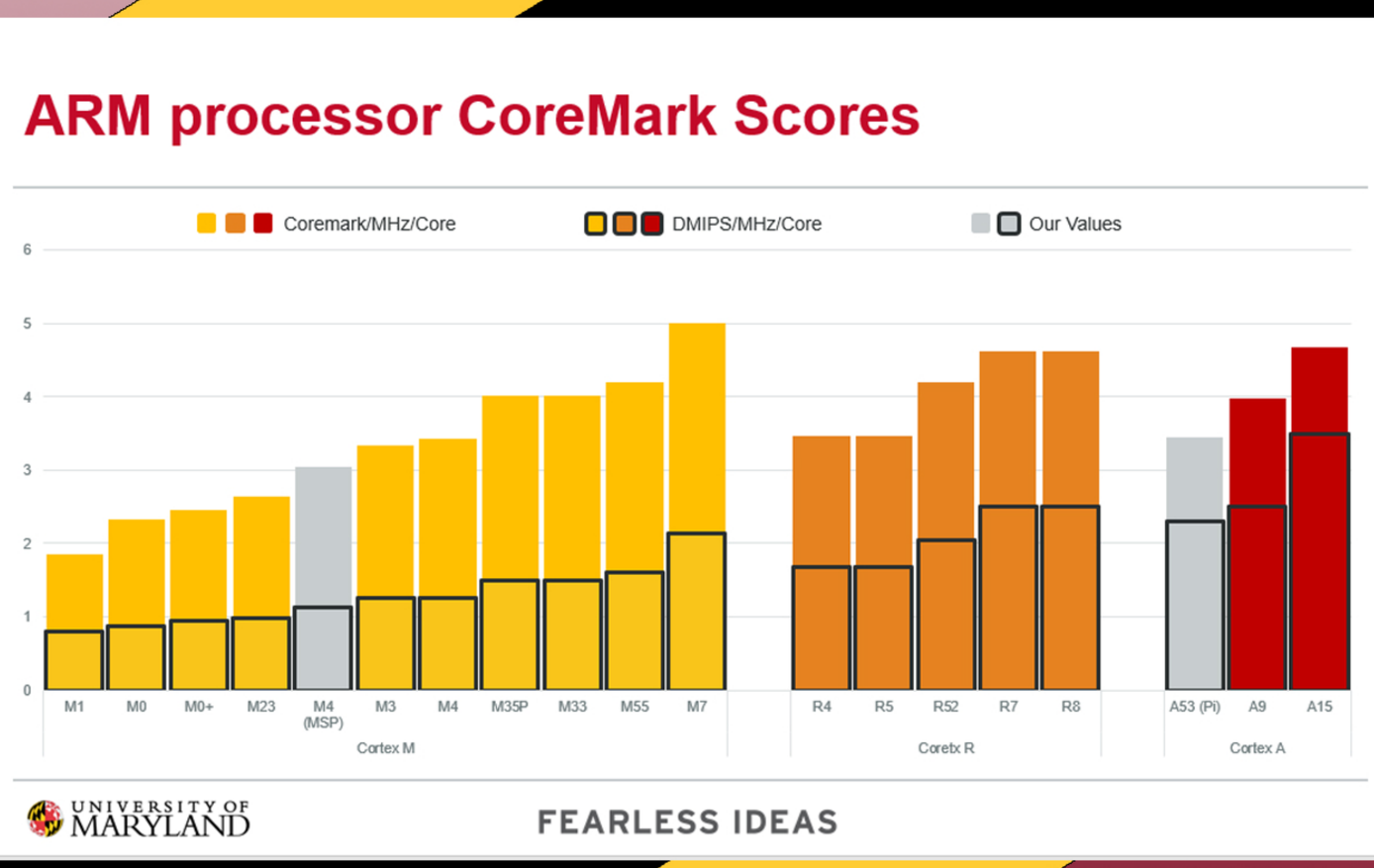
CPSDU

Benchmark	Type	Units	ARM	TI (-o3)	TI (-o4)	gcc (-o3)	gcc (-ofast)
Dhrystone	ground rules	DMIPS/MHz	1.27	1.12	1.05		
	permitting function inlining	DMIPS/MHz	1.55				
	simultaneous compilation	DMIPS/MHz	1.95			1.61	1.61
Whetstone	single precision	KWIPS/MHz		53.12	53.13	77.24	89.8
Coremark			3.42	3.04	3.00	2.57	2.61
GTRACK	2D	Kcycles per track		41.12	28.94	28.33	27.11
GTRACK	3D	Kcycles per track		65.49	44.45	51.22	49.93
Matrix Multiplication	8x8 TI	cycles		6155	2721	7568	7568
	8x8 CMSIS	cycles		6446	4758	6125	6509

Activities:

Not only did I run numerous benchmarks on the M4 (as shown in the table above), but I also distinguished what memory and compiler configurations impacted the preformance of every benchmark. This required me to study and fully comprehend the memory and cache layout of the chip which took me a very long time to research.

I also had to understand the difference between the benchmarks since I needed to make sure that every single different in preformance was accounted for by known factors or constraints.



Implications

The research I did brought a plenthora of interesting factors to light. The most important of these factors is that each benchmarks preformance was decided by how heavily it relied on floating point arithmetic as well as Trigonometry, exponents, and roots. The most important of these discoveries was deffinetly the link I found between the compilers set clock speed and the memory states of the chipset. Basically, 12MHz allows the CPU to work with 0 wait states while 48MHz works with 1 wait state. Finding and proving this conclusion was a lot of work but proved to be very well worth it since it highlighted a huge factor in preformance that was so deep in the architiecture that it would have otherwise been overlooked. When looking at the preformance of this chip we now know to check the compiler version, clock speeds, benchmark specific loads, and hardware like FPU's and support of THUMB-2.

Agknowlegements

I would love to thank my mentor and other Texas Instruments employees for coming up with ways for me to be envolved in large scale projects while also allowing my work to be non-confidential so that I can share it here today. I hope my research is well used in the future and I will deffinetly use the knowlege I gained in future internships.